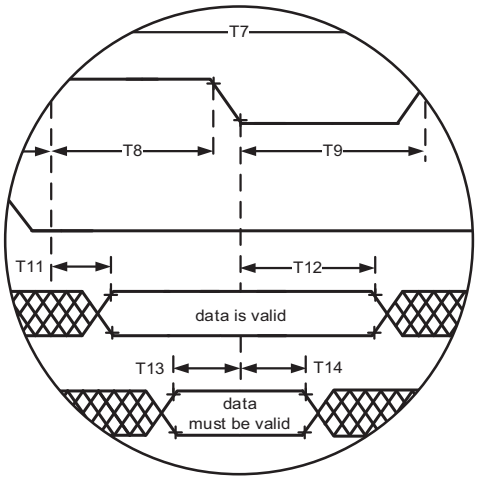
PERFORMANCE MOTION DEVICES
MOTION CONTROL AT ITS CORE



Magellan® Motion Control IC

MC58113 Electrical Specifications

Revision 1.4 / November 2023

Performance Motion Devices, Inc.
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Related Documents

Magellan® Motion Control IC User Guide

Complete description of the Magellan Motion Control IC features and functions with detailed theory of operation.

C-Motion Magellan Programming Reference

Descriptions of all Magellan Motion Control IC commands, with coding syntax and examples, listed alphabetically for quick reference.

MC58113 Developer Kit User Manual

How to install and configure the DK58113 developer kit.

Atlas Digital Amplifier User Manual

Description of the Atlas Digital Amplifier electrical and mechanical specifications along with a summary of its operational features.

Atlas Digital Amplifier Complete Technical Reference

Complete technical and mechanical description of the Atlas Digital Amplifier with detailed theory of operations.

Table of Contents

List of Figures

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1. The MC50000 Family

1

In This Chapter

- Introduction
- Magellan Motion Control IC Family Overview
- MC58113-Series ICs & Developer Kits

1.1 Introduction

This manual describes the electrical characteristics of the MC58113, MC53113, MC51113, and MC54113 motion control IC from PMD. These devices are members of PMD's Magellan IC family.

The MC58113-series ICs are complete chip-based motion controllers. They provide trajectory generation, programmable breakpoints, advanced performance trace, and many related motion control functions. Depending on the type of motor controlled, they provide servo-loop closure, on-board commutation for brushless motors, and pulse and direction output. Finally, the MC58113-series ICs provide advanced digital current control along with numerous amplifier management and safety features.

The MC58113-series ICs together with other Magellan ICs provide a software-compatible family of dedicated motion control ICs which can handle a large variety of system configurations. Having similar hardware and command architecture enable Magellan ICs to share software commands, so that software written for one may be re-used with another; even though the type of motor may be different.

1.2 Magellan Motion Control IC Family Overview

	MC58000 Series (Except MC58113)	MC55000 Series	MC58113 Series
# of axes	1, 2, 3, 4	1, 2, 3, 4	1+ (primary & aux channel encoder input)
Motor types supported	DC Brush, Brushless DC, step motor	Step motor	DC Brush, Brushless DC, step motor
Output format	SPI Atlas, PWM, DAC, pulse & direction	Pulse & direction	SPI Atlas, PWM, DAC, pulse & direction
Parallel host communication	✓	✓	
Serial host communication	✓	✓	✓
CAN 2.0B host communication	✓	✓	✓
SPI host communication			✓
Incremental encoder input	✓	✓	✓
Parallel word device input	✓	✓	
Index & Home signals	✓	✓	✓
Position capture	✓	✓	✓
Directional limit switches	✓	✓	✓

	MC58000 Series (Except MC58113)	MC55000 Series	MC58113 Series
PWM output	✓		✓
Parallel DAC output	✓		
SPI Atlas interface	✓		✓
SPI DAC output	✓		✓
Pulse & direction output	✓	✓	✓
Digital current control	✓ (with Atlas)		✓
Field oriented control	✓ (with Atlas)		✓
Under/overvoltage sense	✓ (with Atlas)		✓
I^2T Current foldback	✓ (with Atlas)		✓
DC Bus shunt resistor control			✓
Overtemperature sense	✓ (with Atlas)		✓
Short circuit sense	✓ (with Atlas)		✓
Trapezoidal profiling	✓	✓	✓
Velocity profiling	✓	✓	✓
S-curve profiling	✓	✓	✓
Electronic gearing	✓	✓	✓
On-the-fly changes	✓	✓	✓
PID position servo loop	✓		✓
Dual biquad filters	✓		✓
Dual encoder loop	✓ (multi-axis configurations only)		✓
Programmable derivative sampling time	✓		✓
Feedforward (accel & vel)	✓		✓
Data trace/diagnostics	✓	✓	✓
Motion error detection	✓	✓ (with encoder)	✓
Axis settled indicator	✓	✓ (with encoder)	✓
Analog input	✓	✓	✓
Programmable bit output	✓	✓	✓
Software-invertible signals	✓	✓	✓
User-defined I/O	✓	✓	
Internal Trace Buffer			✓
External RAM support	✓	✓	
Multi-chip synchronization	✓		✓
Chipset configurations	MC58420 (4 axes, 2 ICs) MC58320 (3 axes, 2 ICs) MC58220 (2 axes, 2 ICs) MC58120 (1 axis, 2 ICs) MC58110 (1 axis, 1 IC)	MC55420 (4 axes, 2 ICs) MC55320 (3 axes, 2 ICs) MC55220 (2 axes, 2 ICs) MC55120 (1 axis, 2 ICs) MC55110 (1 axis, 1 IC)	MC51113 (1+ axis, 1 IC) MC53113 (1+ axis, 1 IC) MC54113 (1+ axis, 1 IC) MC58113 (1+ axis, 1 IC)
IC Package: CP chip	MC58x20: 144 pin TQFP MC58110: 144 pin TQFP	MC55x20: 144 pin TQFP MC55110: 144 pin TQFP	100 pin TQFP
IC Package: IO chip	MC58x20: 100 pin TQFP MC58110: NA	MC55x20: 100 pin TQFP MC55110: NA	N/A

1.3 MC58113-Series ICs & Developer Kits

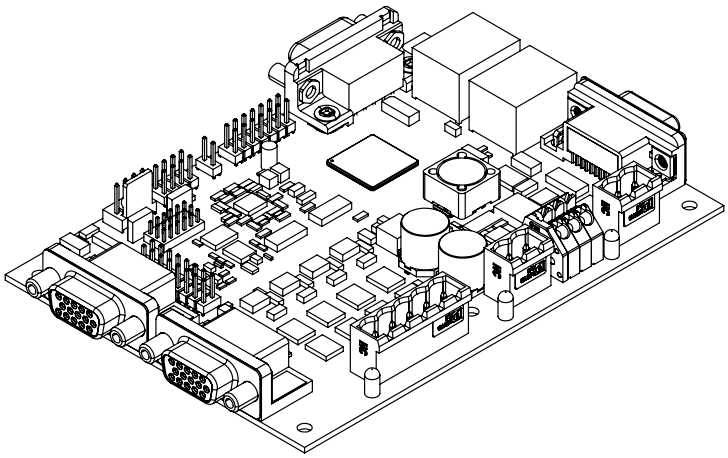

Figure 1-1: DK58113 Board

There are four members of the MC58113-series ICs; MC58113, MC53113, MC51113, and MC54113, each of which support different motor types, or combination of motor types. Developer Kits are available which support each member of the MC58113 IC family, and a socketed version is available which supports all of the MC58113 family ICs: The following table shows this:

IC	Developer Kit p/n	Motors Supported
MC58113	DK58113	DC Brush, Brushless DC, step motor
MC53113	DK53113	Brushless DC
MC51113	DK51113	DC Brush
MC54113	DK54113	Step motor
MC58113	DK58113S	Socketed DK accepts all MC58113 family ICs

All of the above Developer Kit versions share the same physical DK58113 card as well as the same software CD. They differ in the specific type of MC58113-series IC chip that is installed and whether the MC58113 family IC is socketed.

Note that throughout this manual in addition to the MC58113 IC, the term MC58113 may also be used to mean the complete product family; MC58113, MC53113, MC51113, and MC54113.

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2. Functional Characteristics

2

In This Chapter

- Configurations, Parameters, and Performance
- Physical Characteristics and Mounting Dimensions
- Absolute Maximum Environmental and Electrical Ratings
- MC58113-Series ICs Interconnection Overview

2.1 Configurations, Parameters, and Performance

Profile modes	S-curve point-to-point	Position, velocity, acceleration, deceleration, and jerk parameters
	Trapezoidal point-to-point	Position, velocity, acceleration, and deceleration parameters
	Velocity-contouring	Velocity, acceleration, and deceleration parameters
	Electronic Gear	Encoder input, pulse & direction input, or trajectory position of one axis used to drive a second axis. Master and slave axes and gear ratio parameters
Current control modes	A/B	Digital loop provides active current control utilizing leg current analog input
	FOC	Field oriented control loop provides active current control utilizing leg current analog input
	Third leg floating	Hall-based mode drives two of three legs with the third leg floating
	Current Loop Off	Voltage mode control, no current feedback used
Communication modes	SPI (Serial Peripheral Interface) with 16-bit command word size Point to point asynchronous serial Multi-drop asynchronous serial CAN bus 2.0B	
Host SPI frequency range	1.0 MHz - 10.0 MHz	
Serial port baud rate range	1,200 baud to 460,800 baud (1,200, 2,400, 9,600, 19,200, 57,600, 115,200, 230,400, 460,800)	
CAN port transmission rate range	10,000 baud to 1,000,000 baud (10,000, 20,000, 50,000, 125,000, 250,000, 500,000, 800,000, 1,000,000)	
Position range	-2,147,483,648 to +2,147,483,647 counts or steps	
Velocity range	-32,768 to +32,767 counts or steps per cycle with a resolution of 1/65,536 counts or steps per cycle	
Acceleration and deceleration ranges	0 to +32,767 counts or steps per cycle[2] with a resolution of 1/65,536 counts or steps per cycle[2]	
Jerk range	0 to ½ counts or steps per cycle[3] with a resolution of 1/4,294,967,296 counts or steps per cycle[3]	
Electronic gear ratio range	-32,768 to +32,767 with a resolution of 1/65,536 (negative and positive direction)	

Filter modes	Scalable PID + velocity feedforward + acceleration feedforward + bias. Also includes integration limit, settable derivative sampling time, output motor command limiting and two bi-quad filters. Dual encoder feedback mode where auxiliary encoder is used for backlash compensation	
Filter parameter resolution	16 bits	
Position error	32 bits	
Position error tracking	Motion error window	Allows axis to be stopped upon exceeding programmable window
	Tracking window	Allows flag to be set if position error is within a programmable position window
	Axis settled	Allows flag to be set if position error is within programmable position window for a programmable amount of time after trajectory motion is complete
Motor output modes	PWM	20 kHz, 40 kHz, 80 kHz
	SPI DAC	16 bits
	Pulse and direction	1.0 Mpulses/sec maximum
	SPI Atlas	Four-signal SPI interface with 16-bit packet commands and SPI Atlas protocol..
Commutation rate	19.53 kHz	
Current loop rate	19.53 kHz	
Current measurement resolution	12 bits	
PWM resolution	1:2,048 @ 20 kHz 1:1,024 @ 40 kHz 1:512 @ 80 kHz	
Current loop type	P, I (proportional integral) with integral limit	
Current loop resolution	16 bits	
Drive safety functions	Over current detect, over temperature detect, over voltage detect, under voltage detect, I^2t current foldback	
Output limiting	Energy, current, and voltage limit	
NVRAM storage size	1,024 16-bit words	
Microstepping waveform	Sinusoidal	
Microsteps per full step	1 to 256	
Maximum encoder rate	25 Mcounts/sec	
Hall sensor inputs	3 Hall effect inputs	
Cycle time range	51.2 microseconds to 1.048576 seconds	
Multi-chip synchronization	<1 μsec difference between master and slave servo cycle	
Limit switches	1 for each direction of travel	
Position-capture triggers	*Index* and *Home* signals	
Other digital signals	1 *AxisIn* signal, 1 *AxisOut* signal	
Software-invertible signals	*Quad A, Quad B, Index, Home, AxisIn, AxisOut, PositiveLimit, NegativeLimit, HallA, HallB, HallC* (all individually programmable), *Pulse, Direction*	
General purpose analog input	1 12-bit analog input	
RAM internal memory	16,380 words	
Maximum number of simultaneous trace variables	4	
Number of traceable variables	73	

2.2 Physical Characteristics and Mounting Dimensions

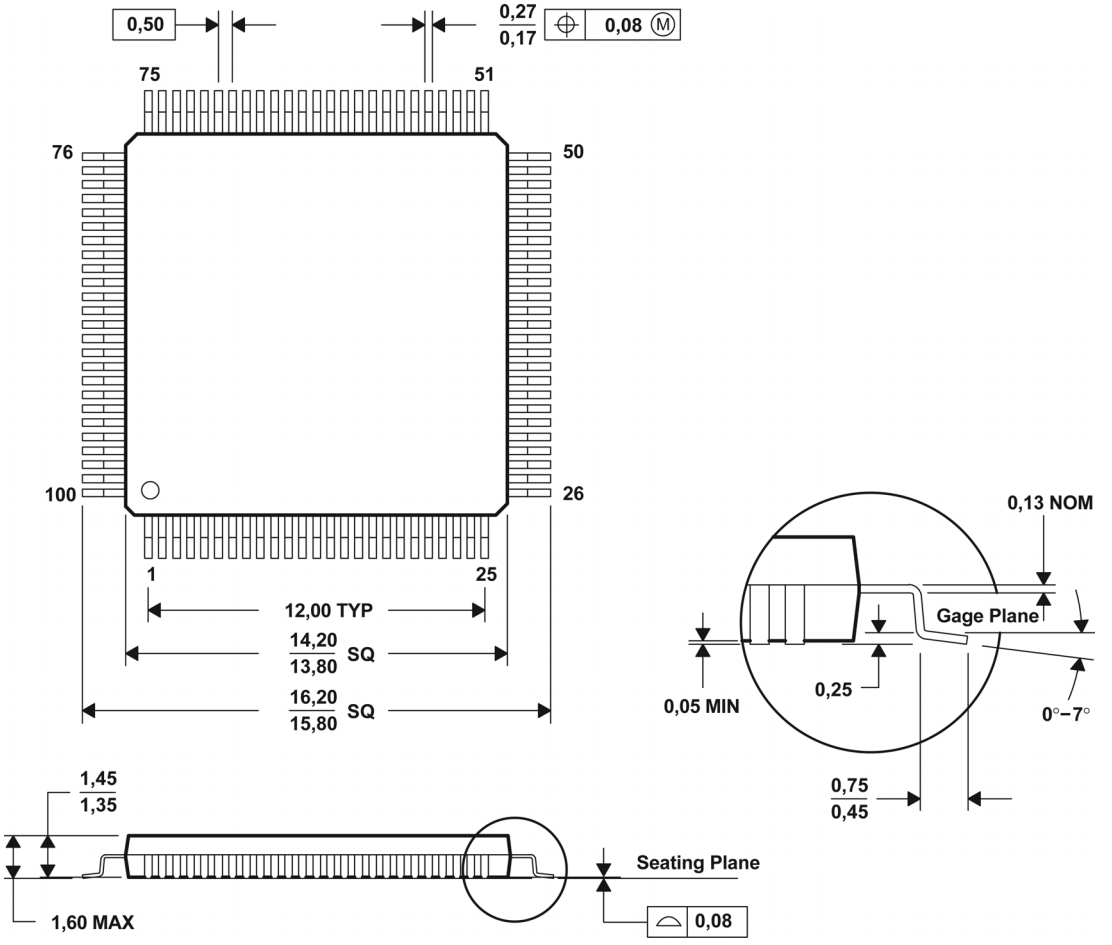

Figure 2-1: MC58113-series ICs Mechanical Dimensions (all dimensions in millimeters)

2.3 Absolute Maximum Environmental and Electrical Ratings[1]

Supply voltage (Vcc)	-0.3V to +4.6V
FltCap pin voltage range	-0.3V to 2.5V
Analog voltage range with respect to AnalogGND (AnalogVcc)	-0.3V to +4.6V
Input voltage (Vi)	-0.3V to +4.6V
Output voltage (Vo)	-0.3V to +4.6V
Input clamp current (Ii,clamp), peak:	+/-20 mA
continuous:	+/-2 mA
Output clamp current (Io,clamp)	+/-20 mA
Package thermal impedance (θ_{JA})	42.2°C/W
Junction temperature range (Tj)[(2)]	-40°C to 150°C
Storage temperature range (Ts)	-65°C to 150°C
Nominal clock frequency (Fclkin)	10.0 MHz

(1) Unless otherwise noted, all voltages are with respect to GND
(2) Please refer to "Design tips" section for more information

2.4 MC58113-Series ICs Interconnection Overview

The following figure shows the principal control and data paths in an MC58113 system.

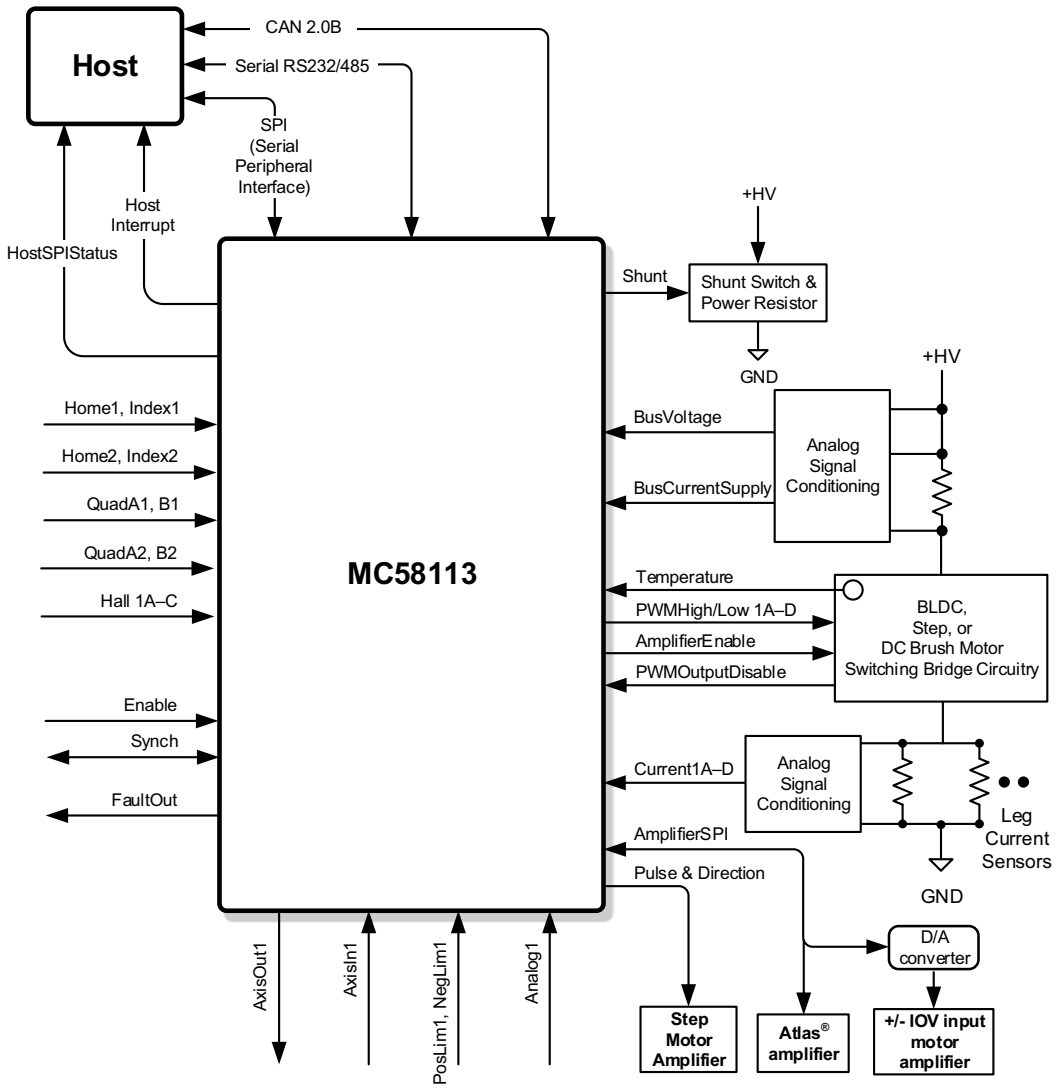

Figure 2-2: MC58113-series ICs Control and Data Paths

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3. Electrical Characteristics

3

In This Chapter

- DC Characteristics for MC58113-Series ICs
- AC Characteristics

3.1 DC Characteristics for MC58113-Series ICs

(Vcc and Ta per operating ratings, Fclkin=10.0MHz)

Symbol	Parameter	Minimum	Maximum	Conditions
V_{cc}	Supply voltage	2.97V	3.63V	With respect to GND
I_{dd}	Supply current		170 mA	All I/O pins are floating
AnalogV_{cc}	Analog input supply voltage	2.97V	3.63V	With respect to AnalogGND
AnalogI_{dd}	Analog supply current		22 mA	
T_a	Operating free-air temperature	-40°C	85°C	Note 2
T_j	Operating junction temperature	-40°C	105°C	
Input Voltage				
V_{ih}	Logic 1 input voltage	2.0V	Vcc+0.3V	
V_{il}	Logic 0 input voltage	-0.3V	0.8V	
Output Voltage				
V_{oh}	Logic 1 Output Voltage	2.4V		Io=-4 mA
		Vcc-0.2V		Io=-50 μA
V_{ol}	Logic 0 Output Voltage		0.4V	Io=4 mA
Other				
I_{out}	Tri-state output leakage current	-2 μA	2 μA	Vo=0 or Vcc
I_{in}	Input current	2 μA	-205 μA	Vcc=3.3V with internal pullup
$I_{in,\sim RESET}$	Input current for ~RESET pin	2 μA	-375 μA	Vcc=3.3V
C_i	Input capacitance		2 pF	typical
V_{fltcap}	FltCap voltage		1.9V	typical
V_{reset}	Vcc BOR trip point	2.50V	2.96V	Falling Vcc
$V_{reset,hys}$	Vcc BOR hysteresis		35 mV	typical
T_{reset}	BOR reset release delay time	400 μs	800 μs	Time from removing reset to ~RESET release
Analog Input				
I_{refhi}	AnalogRefHigh input current		100 μA	typical
$Analog_{RefLow}$	Analog low voltage reference	AnalogGND	0.66V	

Symbol	Parameter	Minimum	Maximum	Conditions
$Analog_{RefHigh}$	Analog high voltage reference	2.64V	AnalogVcc	
		1.98V	AnalogVcc	AnalogRefLow= AnalogGND
V_{analog}	Analog input voltage range	AnalogRefLow	AnalogRefHigh	
C_{ai}	Analog input capacitance		5 pF	typical
E_{dnl}	Differential nonlinearity error. Difference between the step width and the ideal value. No missing codes.	-1	1.5	LSB
E_{inl}	Integral nonlinearity error. Maximum deviation from the best straight line through the ADC transfer characteristics, excluding the quantization error.	-4	4	LSB
E_{zo}	Zero-offset error	-4	4	LSB

Notes:
(1) V_{cc} and $AnalogV_{cc}$ should be within 0.3V from each other.
(2) Please refer to design tips for thermal design considerations.

3.2 AC Characteristics

Refer to Chapter 4, "Timing Diagrams," for timing diagrams.

3.2.1 Clock

Timing Interval	No.	Min	Max
ClkIn frequency, typical			10 MHz
ClkIn period, typical	T1		100 nSec
ClkIn fall time	T2		6 nSec
ClkIn rise time	T3		6 nSec
ClkIn pulse duration		0.45 T1	0.55 T1

3.2.2 Quadrature Encoder Input

Timing Interval	No.	Min	Max
Encoder pulse width	T4	33.3 nSec	
Dwell time per state	T5	16.7 nSec	
~Index active pulse time	T6	33.3 nSec	

Notes:
(1) ~Index is defaulted as active low (trigger occurs upon low to high transition). This interpretation can be reversed via the **SetSignalSense** command.

(2) Capture of the quadrature position at the time of index trigger is guaranteed if the A&B signals remain in the same state for 25 nSec after the trigger event. If the A and B signals change within this time frame the captured position may be the position at time of trigger, or the changed position.

3.2.3 Amplifier SPI in Atlas Mode

Timing Interval	No.	Min	Max
AmplifierSPIClock clock cycle time, typical	T7		250 nSec
Pulse duration, AmplifierSPIClock high	T8	115 nSec	135 nSec
Pulse duration, AmplifierSPIClock low	T9	115 nSec	135 nSec
~AmplifierSPIEnable active to first AmplifierSPIClock high	T10	400 nSec	
AmplifierSPIClock high to AmplifierSPIXmt valid delay time	T11		21 nSec
AmplifierSPIXmt data valid time after AmplifierSPIClock low	T12	40 nSec	
AmplifierSPIRcv setup time before AmplifierSPIClock high	T13	26 nSec	
AmplifierSPIRcv valid time after AmplifierSPIClock low	T14	50 nSec	
Last AmplifierSPIClock low to ~AmplifierSPIEnable inactive	T15	40 nSec	

3.2.4 Amplifier SPI in DAC mode

Timing Interval	No.	Min	Max
AmplifierSPIClock clock cycle time, typical	T16		250 nSec
Pulse duration, AmplifierSPIClock high	T17	115 nSec	135 nSec
Pulse duration, AmplifierSPIClock low	T18	115 nSec	135 nSec
~AmplifierSPIEnable active to first AmplifierSPIClock high	T19	400 nSec	
AmplifierSPIClock high to AmplifierSPIXmt valid delay time	T20		21 nSec
AmplifierSPIXmt data valid time after AmplifierSPIClock low	T21	40 nSec	
Last AmplifierSPIClock low to ~AmplifierSPIEnable inactive	T22	40 nSec	

3.2.5 Host SPI

Timing Interval	No.	Min	Max
HostSPIClock clock cycle time	T23	80 nSec	
Pulse duration, HostSPIClock high	T24	24 nSec	
Pulse duration, HostSPIClock low	T25	24 nSec	
~HostSPIEnable low to first HostSPIClock high	T26	18.8 nSec	
HostSPIClock high to HostSPIXmt valid delay time	T27		21 nSec
HostSPIXmt data valid time after HostSPIClock low	T28	T25	
HostSPIRcv setup time before HostSPIClock high	T29	18.8 nSec	
HostSPIRcv valid time after HostSPIClock low	T30	18.8 nSec	
Last HostSPIClock low to ~HostSPIEnable high	T31	18.8 nSec	

3.2.6 Power-on Reset

Timing Interval	No.	Min	Max
Power on pulse duration driven by device (typical)(note 1)	T32		600 μSec
Device ready/ outputs initialized (typical)	T33		2 mSec
ClkIn ready to ~Reset release	T34	0	

Notes:

(1) The device will generate ~*Reset* pulse upon power on, and external ~*Reset* signal is optional.

(2) During power up and after reset, pin 87, 86, 84, 83, 9, 10, 58, 57, 54, 74, 73, 41, 40, 82, 76, 1, 8, 56 and 94 are in high-impedance, and the rest of I/O pins act as input with weak pull-up.

3.2.7 Warm Reset

Timing Interval	No.	Min	Max
~Reset low duration for warm reset	T35	32 T1	

4. Timing Diagrams

4

In This Chapter

- Clock
- Quadrature Encoder Input
- SPI Atlas Timing
- SPI DAC Timing
- Host SPI Timing
- Power On Timing
- Warm Reset

For the values of *Tn*, please refer to the table in Section 3.2, "AC Characteristics," for more information

4.1 Clock

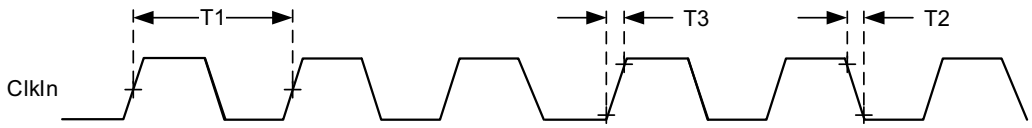


Figure 4-1: Clock Timing

4.2 Quadrature Encoder Input

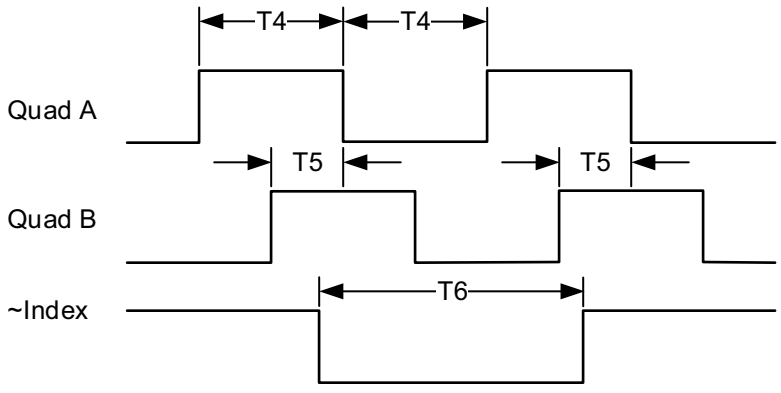
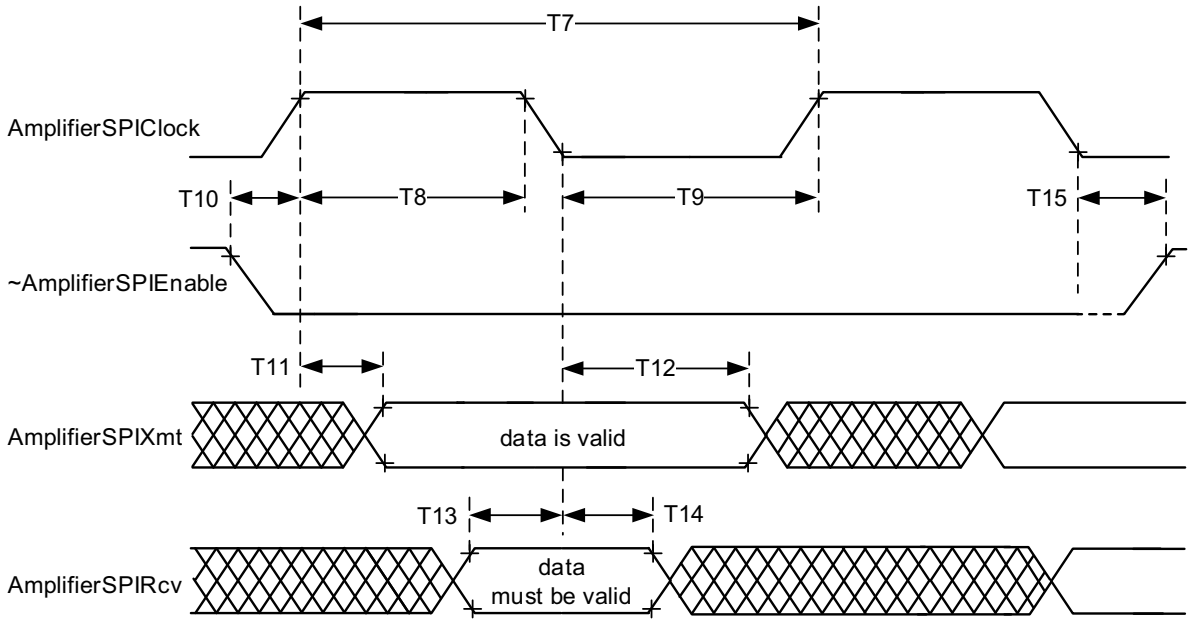


Figure 4-2: Quad Encoder Timing

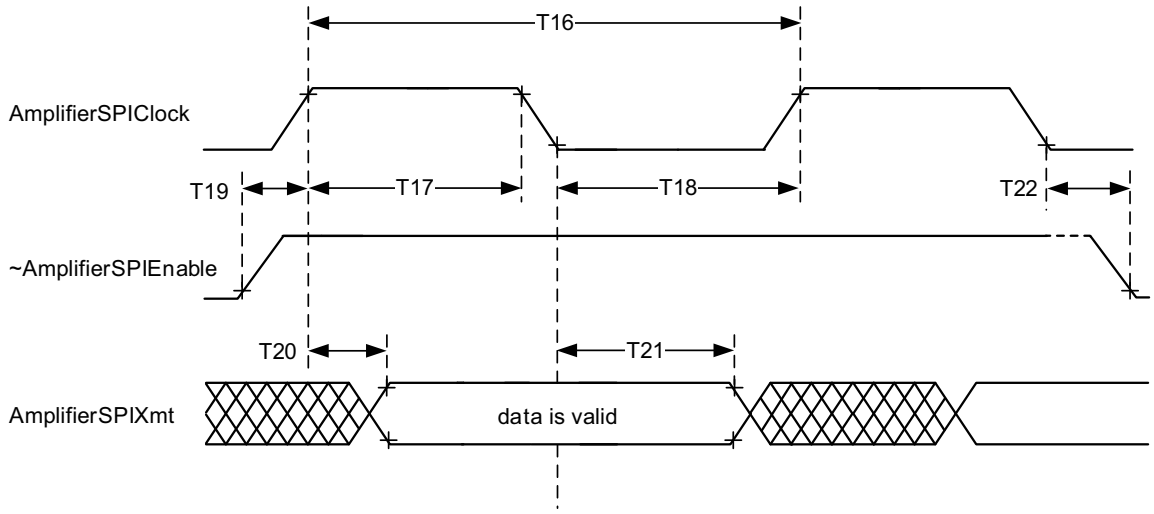
4.3 SPI Atlas Timing

Figure 4-3: SPI Atlas Timing



4.4 SPI DAC Timing

Figure 4-4: SPI DAC Timing



4.5 Host SPI Timing

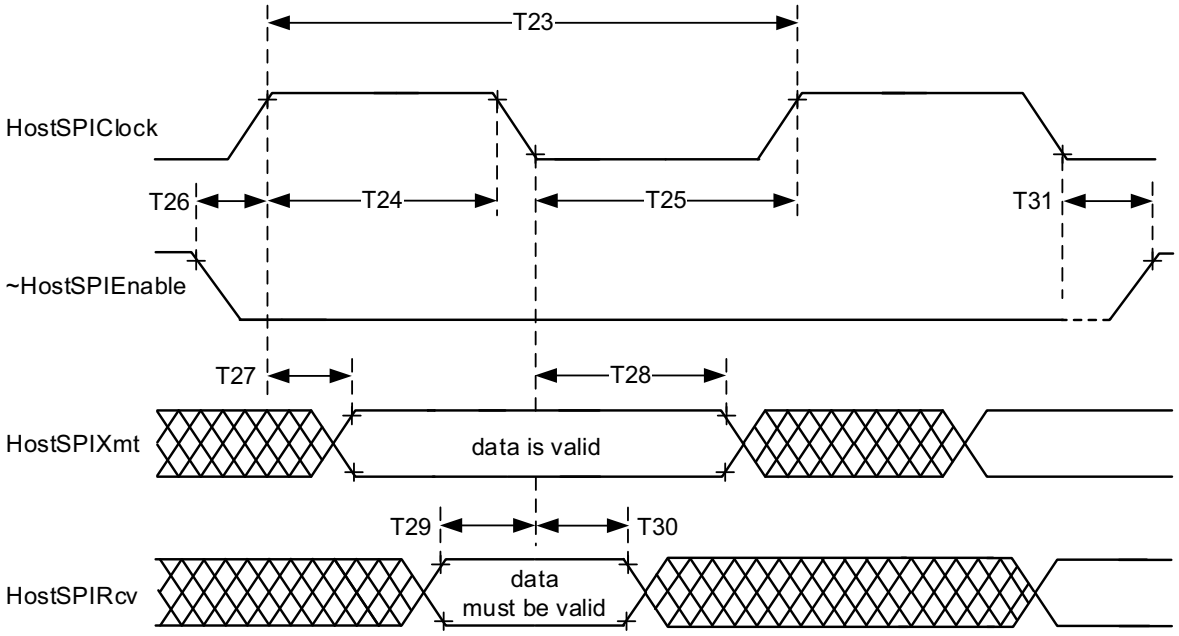


Figure 4-5: Host SPI Timing

4.6 Power On Timing

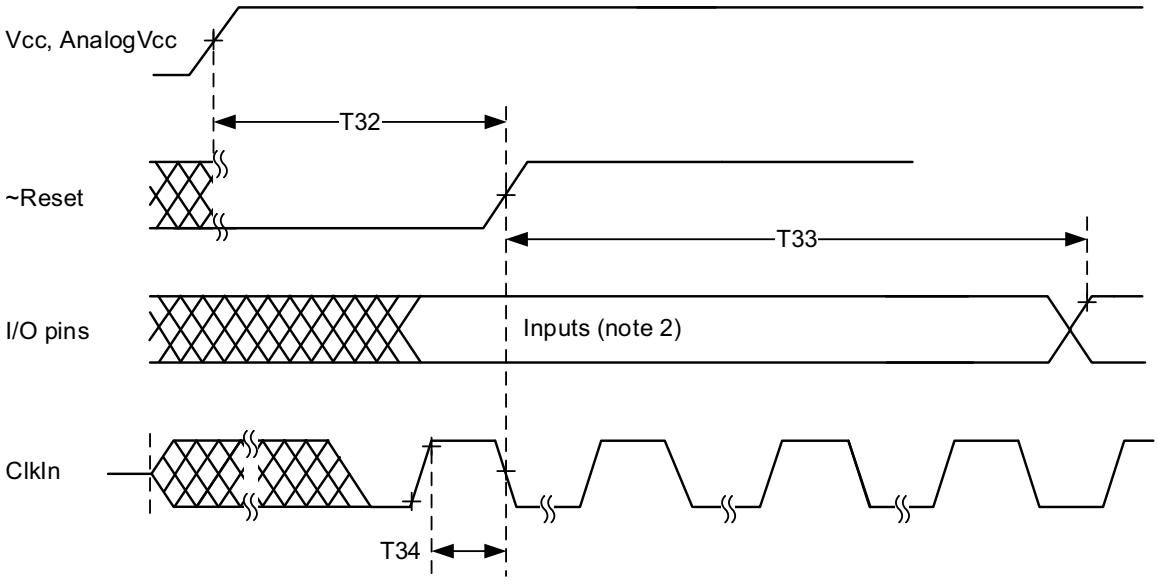
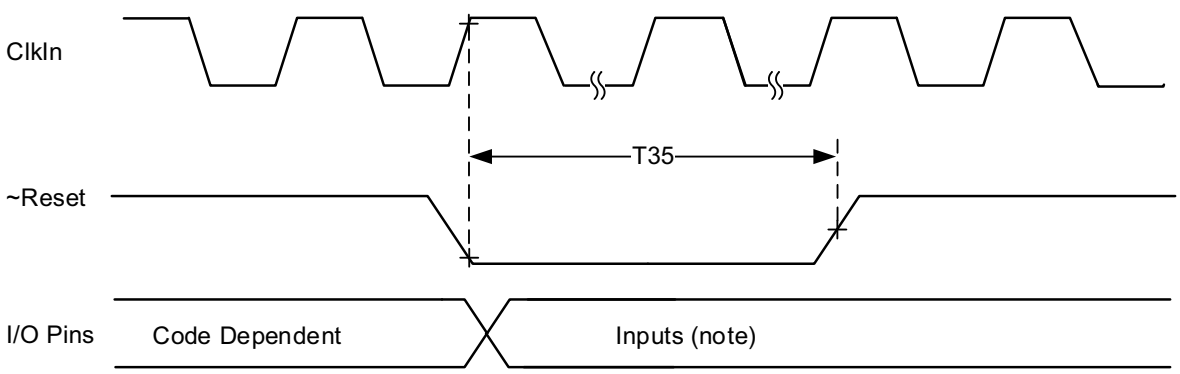


Figure 4-6: Power On Timing

Please refer to Note 2 in Section 3.2.6, "Power-on Reset."

4.7 Warm Reset

Figure 4-7: Warm Reset Timing



Please refer to Note 2 in Section 3.2.7, "Warm Reset."

5. Pinouts and Pin Descriptions

5

In This Chapter

- Pinouts for the MC58113
- Pinouts for the MC51113
- Pinouts for the MC53113
- Pinouts for the MC54113
- MC58113-Series ICs Pin Descriptions

5.1 Pinouts for the MC58113

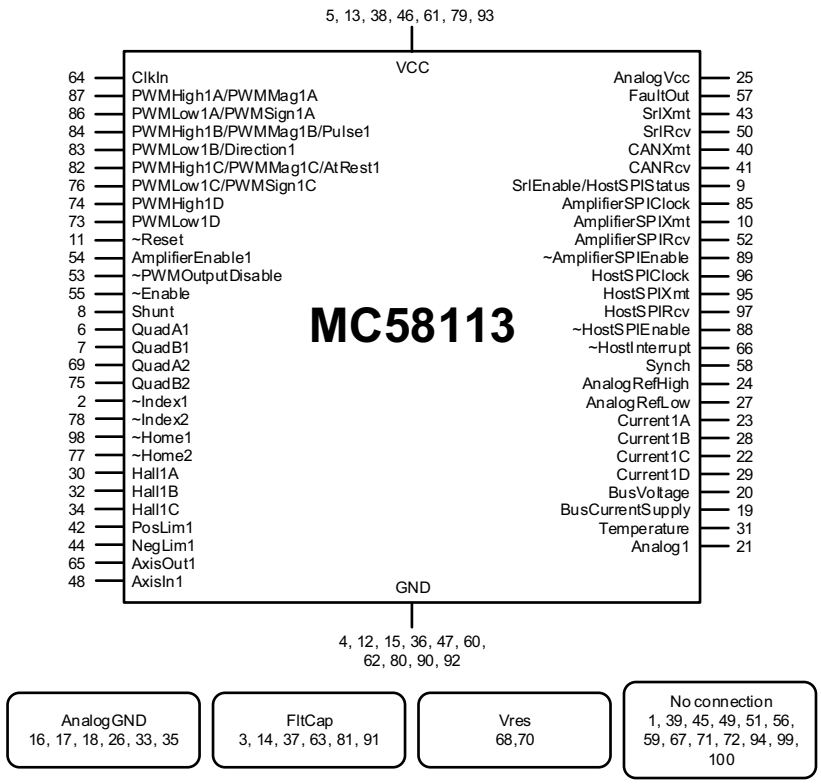
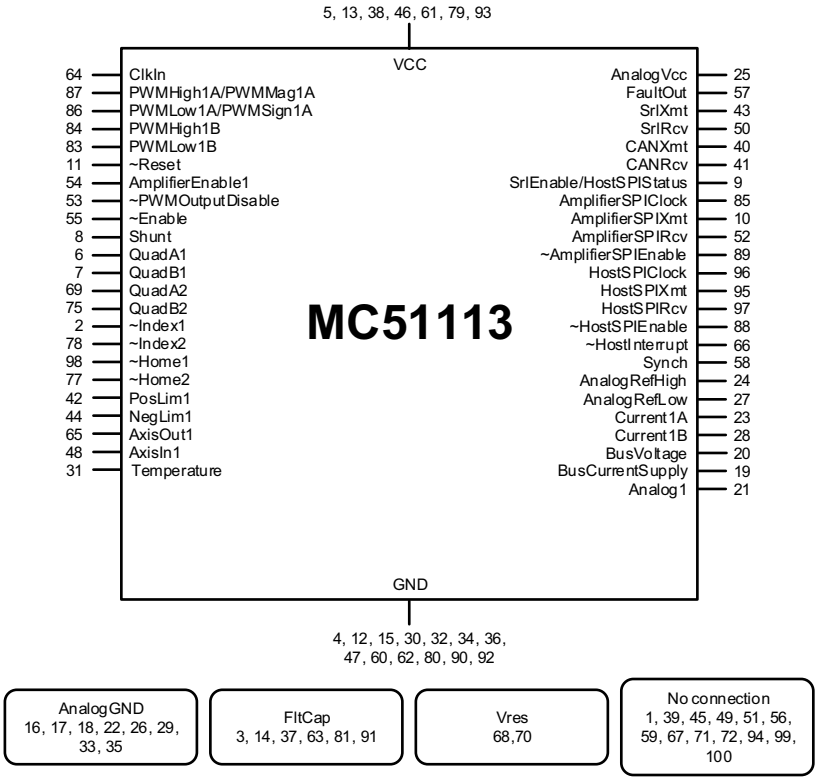


Figure 5-1: MC58113 Pinouts

5.2 Pinouts for the MC51113

Figure 5-2: MC51113 Pinouts



5.3 Pinouts for the MC53113

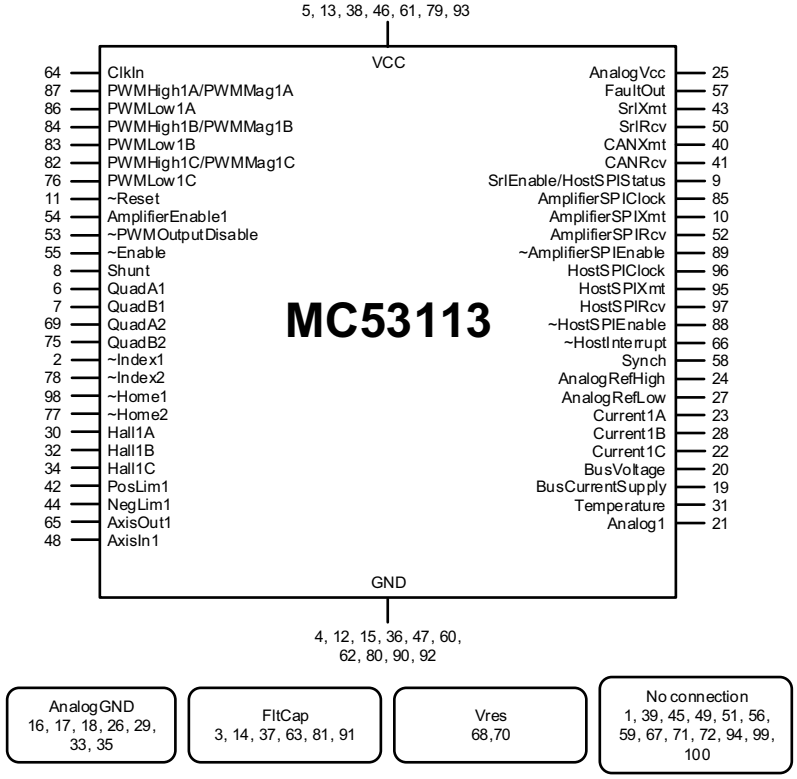
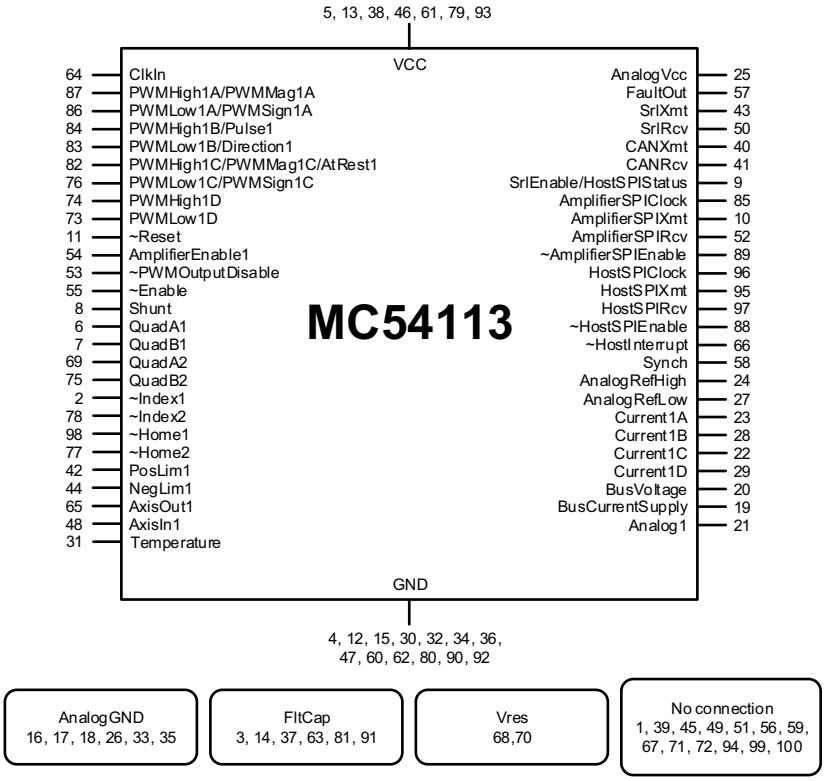


Figure 5-3: MC53113 Pinouts

5.4 Pinouts for the MC54113

Figure 5-4: MC54113 Pinouts



5.5 MC58113-Series ICs Pin Descriptions

MC58113-Series ICs			
Pin Name	#	**Direction**	**Description**
~Reset	11	input	This pin is the master reset input. It may be temporarily brought low to reset the MC58113 to its initial conditions and then restored to high for normal operation. If driven, this pin must be driven by an open-drain device. During powerup it is not necessary to provide a reset. The MC58113 generates an internal reset upon powerup. For correct reset operation a 10k pull-up resistor should be added between Reset and Vcc. In addition, a 100nF or smaller capacitor is recommended between Reset and GND for noise filtering.
ClkIn	64	input	This pin is the master clock input. It is driven at a nominal 10 MHz using an external clock.
PWMHigh1A/ PWMMag1A PWMLow1A/ PWMSign1A PWMHigh1B/ PWMMag1B/Pulse1 PWMLow1B/ Direction1 PWMHigh1C/ PWMMag1C/ AtRest1 PWMLow1C/ PWMSign1C PWMHigh1D PWMLow1D	87 86 84 83 82 76 74 73	output	Depending upon the selected motor type and output mode, these pins have the following functions: *PWMHigh1A/B/C/D* signals encode the high side drive for a switching bridge with separate high/low controls. The default encoding is active high, however this can be changed using the **SetDrivePWM** command. *PWMLow1A/B/C/D* signals encode the low side drive for a switching bridge with separate high/low controls. The default encoding is active high, however this can be changed using the **SetDrivePWM** command. *PWMMag1A/B/C* signals encode the magnitude of a pulse width modulated output for use with switching bridges with magnitude/sign controls or level-encoded controls. The default encoding is active high, however this can be changed using the **SetDrivePWM** command. *PWMSign1A/C* signals encode the sign of the pulse width modulated output for use with switching bridges with magnitude/sign controls. *Pulse1* provides a pulse (step) signal to a pulse & direction amplifier. A step occurs when the signal transitions from a high state to a low state. This default behavior can be changed from a low to a high state transition using the command **SetSignalSense**. *Direction1* indicates the direction of motion, and works in conjunction with the *Pulse* signal. A high level on this signal indicates a positive direction move, and a low level indicates a negative direction move. *AtRest1* indicates that the axis is at rest, and that the step motor can be switched to low power or standby. A high level on this signal indicates the axis is at rest. A low signal indicates the axis is in motion.
AmplifierEnable	54	output	This pin provides an amplifier enable signal that may be useful for some amplifier connection schemes. A high signal indicates that amplifier output should be enabled and a low indicates that amplifier output should be disabled.
~PWMOutputDisable	53	input	This pin inputs a high speed PWM output disable that may be useful for safety protection with some PWM amplifier schemes. When low, PWM output is disabled. PWM operation is normal when this signal is high.
~Enable	55	input	This pin is an enable input. To allow normal operations a low signal is asserted. When a high signal is asserted motor control operations are disabled, although communications and various other operations are still available.

MC58113-Series ICs			
Pin Name	**#**	**Direction**	**Description**
Shunt	8	output	This pin provides a PWM-based shunt signal that may be used with an external switching circuit and high wattage resistor or other energy dissipating device to regulate supply bus overvoltage conditions.
QuadA1 QuadB1 QuadA2 QuadB2	6 7 69 75	input	These pins input the A and B quadrature signals for the incremental encoder for the primary axis (axis 1) and the auxiliary axis (axis 2). By default, when the axis is moving in the positive (forward) direction, signal A leads signal B by 90°, however both the *QuadA* and *QuadB* signal interpretation can be changed via the command **SetSignalSense**. **Note:** Some encoders require a pull-up resistor to 3.3V on each signal to establish a proper high signal. Check your encoder's electrical specification. These signals may also be used to input a pulse and direction datastream, with the pulse and direction inputs connected to the *QuadA1* and *QuadB1* signals respectively or the *QuadA2* and *QuadB2* signals respectively. See the **SetEncoderSource** command for more information. If unused, these pins may be left unconnected.
~Index1 ~Index2	2 78	input	These pins input the index signals for the corresponding incremental encoders. By default a valid index pulse is recognized when *~Index* transitions low, however the interpretation of this signal can be changed via the command **SetSignalSense**. For axis 1 the user can select either the *Index1* or *Home1* signal as the hardware capture source. For axis 2 (the auxiliary encoder input) *Home2* is always the hardware capture source. The *Index2* signal can be used for phase correction of Brushless DC motors when the position loop is operated in dual loop servo mode. **Note:** Index capture is not conditioned by the *QuadA* and *QuadB* signals. If such conditioning is not provided by the encoder then external circuitry should be used if such conditioning is desired. If unused, these pins may be left unconnected.
~Home1 ~Home2	98 77	input	These pins input home signals, which are general-purpose inputs to the axis specific position-capture mechanism. By default, a valid home signal is recognized when *~Home* goes low, however this interpretation can be changed via the command **SetSignalSense**. If unused, these pins may be left unconnected.
Hall1A Hall1B Hall1C	30 32 34	input	These pins input Hall-encoded phasing inputs for brushless DC motors. The A, B, and C signals encode six valid states as follows: A on, A and B on, B on, B and C on, C on, C and A on. By default a sensor is defined as being on when its signal is high, however this signal interpretation can be changed via the command **SetSignalSense**. **Note:** Some Hall sensors require a pull up resistor to 3.3V on each signal to establish a proper high signal. Check your Hall sensor's electrical specification. If unused, these pins may be left unconnected.
PosLim1	42	input	This pin inputs a positive-side (forward) travel limit switch signal. By default this signal has active low interpretation, however this interpretation can be changed using the command **SetSignalSense**. If unused this pin may be left unconnected.
NegLim1	44	input	This pin inputs a negative-side (reverse) travel limit switch signal. By default this signal has active low interpretation, however this interpretation can be changed using the command **SetSignalSense**. If unused this pin may be left unconnected.

MC58113-Series ICs			
Pin Name	#	**Direction**	**Description**
AxisOut1	65	output	This pin can be programmed to track the state of any bit in the MC58113's internal status registers. The interpretation of this signal output can be changed via the command **SetSignalSense**.
AxisIn1	48	input	This pin is a general purpose input which can also be used as a breakpoint input. The interpretation of this signal input can be changed via the command **SetSignalSense**. If unused, this pin may be left unconnected.
FaultOut	57	output	This pin provides a general purpose fault indicator that can be programmed to indicate a number of conditions including a motion error, amplifier error, or various other conditions. A high indicates that a fault condition is present.
SrlXmt	43	output	This pin outputs serial data from the asynchronous serial port.
SrlRcv	50	input	This pin inputs serial data to the asynchronous serial port. If unused, this pin may be left unconnected.
CANXmt	40	output	This pin transmits serial data to the CAN transceiver.
CANRcv	41	input	This pin inputs serial data from the CAN transceiver. If unused, this pin may be left unconnected.
SrlEnable/ HostSPIStatus	9	output	This pin sets the serial port enable line. *SrlEnable* is high during transmission for the multi-drop protocol, and always high during point–to-point mode. *HostSPIStatus* indicates when the MC58113 has a command result that is ready to be read by the host. A low signal indicates that the command result is ready. This pin supports only one of these two functions at a time. The default function of this pin is *HostSPIStatus*. If serial multi-drop communication is specified via the **SetSerialPortMode** command the function changes to *SrlEnable*.
AmplifierSPIClock	85	output	This pin outputs the clock signal used with synchronous serial transfers on the amplifier SPI bus to DACs or to Atlas amplifiers. During power-up this pin floats temporarily.
AmplifierSPIXmt	10	output	This pin transmits synchronous serial data on the amplifier SPI bus to DACs or to Atlas amplifiers.
AmplifierSPIRcv	52	input	This pin inputs synchronous serial data for the amplifier SPI bus. If unused, this pin may be left unconnected.
~AmplifierSPIEnable	89	output	This pin provides the enable signal when SPIAtlas or SPI DAC motor output modes are used. This signal is active low for SPI Atlas mode, meaning it is low when an SPI Atlas communication is occurring, and high at all other times. This signal is active high for SPI DAC mode, meaning it is high when the SPI DAC channel is being written to, and low at all other times.
HostSPIClock	96	input	This pin inputs the clock signal used with synchronous serial transfer on the host communication SPI bus. If unused, this pin may be left unconnected.
HostSPIXmt	95	output	This pin, also commonly referred to as MISO, transmits synchronous serial data on the host communication SPI bus to the host processor.
HostSPIRcv	97	input	This pin, also commonly referred to as MOSI, inputs synchronous serial data for the host communication SPI bus. If unused, this pin may be left unconnected.
~HostSPIEnable	88	input	This pin inputs an enable signal for the host communication SPI bus. This signal is active low, meaning it should be low when an SPI host communication is occurring, and high at all other times. If unused, this pin may be left unconnected.
~HostInterrupt	66	output	This pin provides a host interrupt signal. When low, it signals an interrupt to the host processor.

MC58113-Series ICs			
Pin Name	**#**	**Direction**	**Description**
Synch	58	input/ output	This pin inputs or outputs a synchronization signal that can be used to synchronize the loop rates of multiple MC58113s with each other, with other Magellan ICs, or with an external source. If unused, this pin may be left unconnected.
AnalogRefHigh	24	input	This pin provides the analog high voltage reference for analog input. The allowed range is 2.0V to *AnalogVcc* . Furthermore, the difference between *Vcc* and *AnalogVcc* should not be larger than 0.3V. If the analog input circuitry is not used, this pin should be tied to *Vcc*.
AnalogRefLow	27	input	This pin provides the analog low voltage reference for analog input. The allowed range is *AnalogGND* to *AnalogRefHigh*. If the analog input circuitry is not used, this pin should be tied to *GND*.
Current1A Current1B Current1C Current1D	23 28 22 29	input	These pins input analog voltages representing leg current flow through the low sides of the switching bridges. DC Brush motors use the A and B inputs, Brushless DC motors use the A, B, and C inputs, and two-phase step motors use the A, B, C, and D inputs. These signals are only accessible when the PWM output mode is set to PWM High/ Low or 50/50 PWM. These signals are used when a current loop is used or when I2t current monitoring is desired. These signals are sampled by an internal A/D converter. The A/D resolution is 12 bits. The allowed signal input range is *AnalogRefLow* to *AnalogRefHigh*. If unused, these signals should be connected to *AnalogGND*.
BusVoltage	20	input	This pin inputs an analog voltage representing the DC bus voltage. The allowed signal input range is *AnalogRefLow* to *AnalogRefHigh*. If unused, this signal should be connected to *AnalogGND*.
BusCurrentSupply	19	input	This pin inputs an analog voltage representing the current through the supply terminal of the DC bus. The allowed signal input range is *AnalogRefLow* to *AnalogRefHigh*. If unused, this signal should be connected to *AnalogGND*.
Temperature	31	input	This pin inputs an analog voltage representing the temperature of the amplifier or other monitored circuitry. The allowed signal input range is *AnalogRefLow* to *AnalogRefHigh*. If unused, this signal should be connected to *AnalogGND*.
Analog1	21	input	This pin inputs an analog voltage representing an uncommitted general purpose input. It may be used to read the voltage level of a user-defined analog signal. The allowed signal input range is *AnalogRefLow* to *AnalogRefHigh*. If unused, this signal should be connected to *AnalogGND*.
AnalogVcc	25		This pin is connected to the analog input supply voltage, which must be in the range of 3.0V to 3.6V. If the analog input circuitry is not used, this pin should be tied to Vcc.
AnalogGND	16, 17, 18, 26, 33, 35		These pins should be connected to the analog input power supply return. Any unused analog inputs (*Current1A-D*, *BusVoltage*, *BusCurrentSupply*, *Temperature* or *Analog1* pins) should be tied to *AnalogGND*.
FltCap	3, 14, 37, 63, 81, 91		Each of these pins must be connected to a 1.2 µF (or higher) filtering capacitor which in turn connects to GND.
Vres	68, 70		Each of these pins must be connected to Vcc via a 10k resistor.
Vcc	5, 13, 38, 46, 61, 79, 93		All of these pins must be connected to the MC58113 digital supply voltage, which should be in the range of 3.0V to 3.6V.
GND	4, 12, 15, 36, 47, 60, 62, 80, 90, 92		All of these pins must be connected to the digital power supply return.

MC58113-Series ICs			
Pin Name	**#**	**Direction**	**Description**
Not connected	1, 39, 45, 49, 51, 56, 59, 67, 71, 72, 94, 99, 100		These pins must be left unconnected.

5.5.1 MC58113-Series ICs Motor-Specific Output Pin Assignments

If the output mode is set to **PWM High/Low**, the following table shows the signals that are used with each motor type.

Brushless DC Signal	Pin	DC Brush Signal	Pin	Step Motor Signal	Pin
PWMHigh1A	87	PWMHigh1A	87	PWMHigh1A	87
PWMLow1A	86	PWMLow1A	86	PWMLow1A	86
PWMHigh1B	84	PWMHigh1B	84	PWMHigh1B	84
PWMLow1B	83	PWMLow1B	83	PWMLow1B	83
PWMHigh1C	82			PWMHigh1C	82
PWMLow1C	76			PWMLow1C	76
				PWMHigh1D	74
				PWMLow1D	73

If the output mode is set to **50/50 PWM**, the following table shows the signals that are used with each motor type.

Brushless DC Signal	Pin	DC Brush Signal	Pin	Step Motor Signal	Pin
PWMMag1A	87	PWMMag1A	87	PWMMag1A	87
PWMMag1B	84			PWMMag1C	82
PWMMag1C	82				

If the output mode is set to **sign/magnitude PWM**, the following table shows the signals that are used with each motor type.

Brushless DC Signal	Pin	DC Brush Signal	Pin	Step Motor Signal	Pin
N/A		PWMMag1A	87	PWMMag1A	87
		PWMSign1A	84	PWMMag1C	82
				PWMSign1A	86
				PWMSign1C	76

If the output mode is set to **Pulse and direction**, the following pinouts should be used.

Signal	Pin
Pulse1	84
Direction1	83
AtRest1	82

If the output mode is set to **SPI DAC**, the following pinouts should be used. SPI DAC output is used with DC Brush motors only.

Signal	Pin
AmplifierSPIEnable	89
AmplifierSPIClock	85
AmplifierSPIXmt	10

If the output mode is set for **SPI Atlas**, which is the interface used with PMD's Atlas Digital Amplifiers, the following pinouts should be used. SPI Atlas can support Brushless DC, DC Brush, and step motors.

Signal	Pin
AmplifierSPIClock	85
AmplifierSPIXmt	10
AmplifierSPIRcv	52
AmplifierSPIEnable	89

6. Additional Electrical Information

6

In This Chapter

- MC58113 Internal Block Diagram
- Switching Motor Amplifier with Current Control
- Overtemperature Protection
- DC Bus Management
- Analog Input Signals
- Multi-chip Synchronization
- MC58113 Memory Buffers
- Output Signal Status During Powerup

6.1 MC58113 Internal Block Diagram

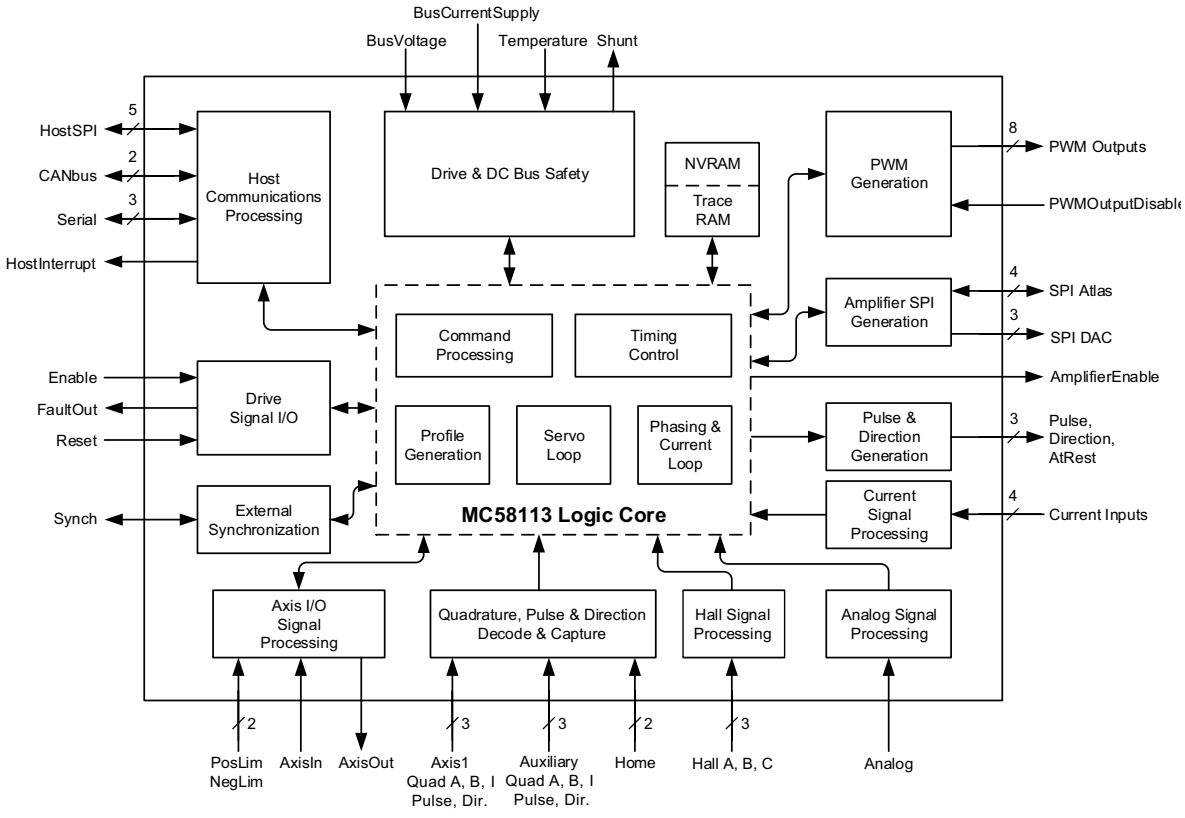


Figure 6-1: MC58113 Series ICs Internal Block Diagram

Figure 6-1 shows the internal block diagram for the MC58113-series ICs.

In the following sections selected portions of the electrical behavior of the MC58113 are detailed.

For a general description of the MC58113-series ICs see the *Magellan Motion Control IC User Guide*. For detailed information on commands supported by the MC58113 ICs see the *C-Motion Magellan Programming Reference*.

6.2 Switching Motor Amplifier with Current Control

The next several sections describe how to connect and set up the MC58113 for operation of a switching amplifier bridge with current control. For electrical information on using the MC58113 with other amplifier configurations see the *Magellan Motion Control IC User Guide* and Sections 7.13 - 7.16 of this manual.

The MC58113-series ICs can control high-efficiency MOSFET or IGBT power stages with PWM input control and leg current feedback. A different configuration is used for each motor type:

- DC Brush motors are driven in an H-Bridge configuration consisting of 4 switches and 2 leg current sensors
- Brushless DC motors are driven in a 3-phase bridge configuration consisting of 6 switches and 3 leg current sensors
- Step motors are driven with two H-Bridges, one for each phase, for a total of 8 switches and 4 leg current sensors

The use of 3-phase and H-Bridge topologies provides full 4-quadrant operation.

6.2.1 Brushless DC Motor Drive

Figure 6-2 shows the typical amplifier stage arrangement when the MC53113 IC is used or when the MC58113 IC is used with Brushless DC motor type selected.

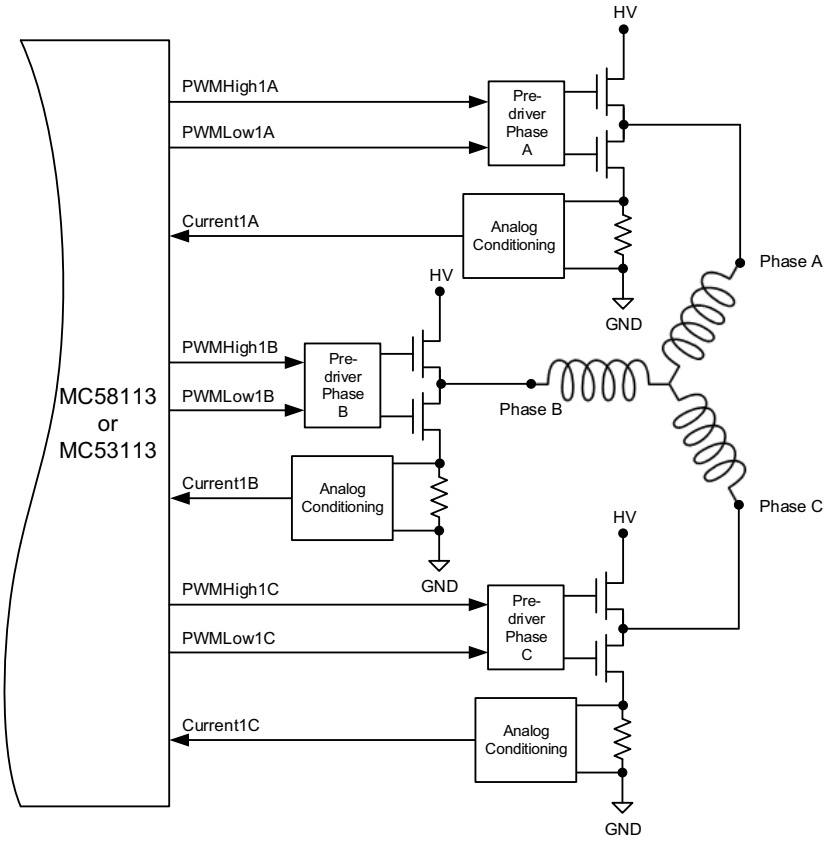


Figure 6-2: Brushless DC Motor Bridge Configuration

6.2.1.1 Brushless DC Amplifier Connections

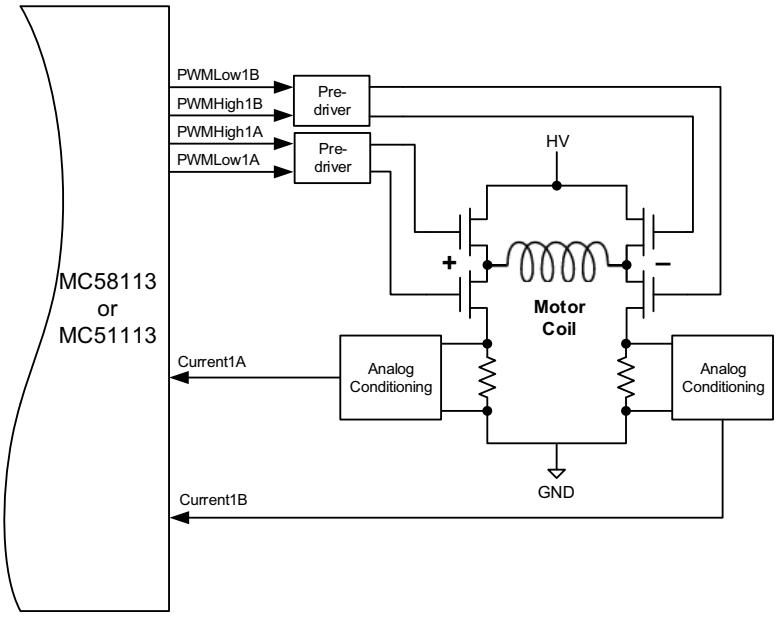
As shown in the table below six PWM output signals and three analog feedback signals interface between the MC58113 IC and the switching amplifier circuitry.

MC58113 signal	Description
PWMHigh1A	Digital high side drive output for motor phase A
PWMLow1A	Digital low side drive output for motor phase A
PWMHigh1B	Digital high side drive output for motor phase B
PWMLow1B	Digital low side drive output for motor phase B
PWMHigh1C	Digital high side drive output for motor phase C
PWMLow1C	Digital low side drive output for motor phase C
Current1A	Analog input containing the current flow through the low side of the switching bridge for phase A.
Current1B	Analog input containing the current flow through the low side of the switching bridge for phase B.
Current1C	Analog input containing the current flow through the low side of the switching bridge for phase C.

6.2.2 DC Brush Motor Drive

Figure 6-3 shows the typical amplifier stage arrangement when the MC51113 IC is used or when the MC58113 IC is used with DC Brush motor type selected.

Figure 6-3: DC Brush Motor Bridge Configuration



6.2.2.1 DC Brush Amplifier Connections

As shown in the table below four PWM output signals and two analog feedback signals interface between the MC58113 IC and the switching amplifier circuitry.

MC58113 signal	Description
PWMHigh1A	Digital high side drive output for the positive coil terminal
PWMLow1A	Digital low side drive output for the positive coil terminal
PWMHigh1B	Digital high side drive output for the negative coil terminal
PWMLow1B	Digital low side drive output for the negative coil terminal
Current1A	Analog input containing the current flow through the positive leg of the bridge
Current1B	Analog input containing the current flow through the negative leg of the bridge

6.2.3 Step Motor Drive

Figure 6-4 shows the typical amplifier stage arrangement when the MC54113 IC is used or when the MC58113 IC is used with step motor type selected

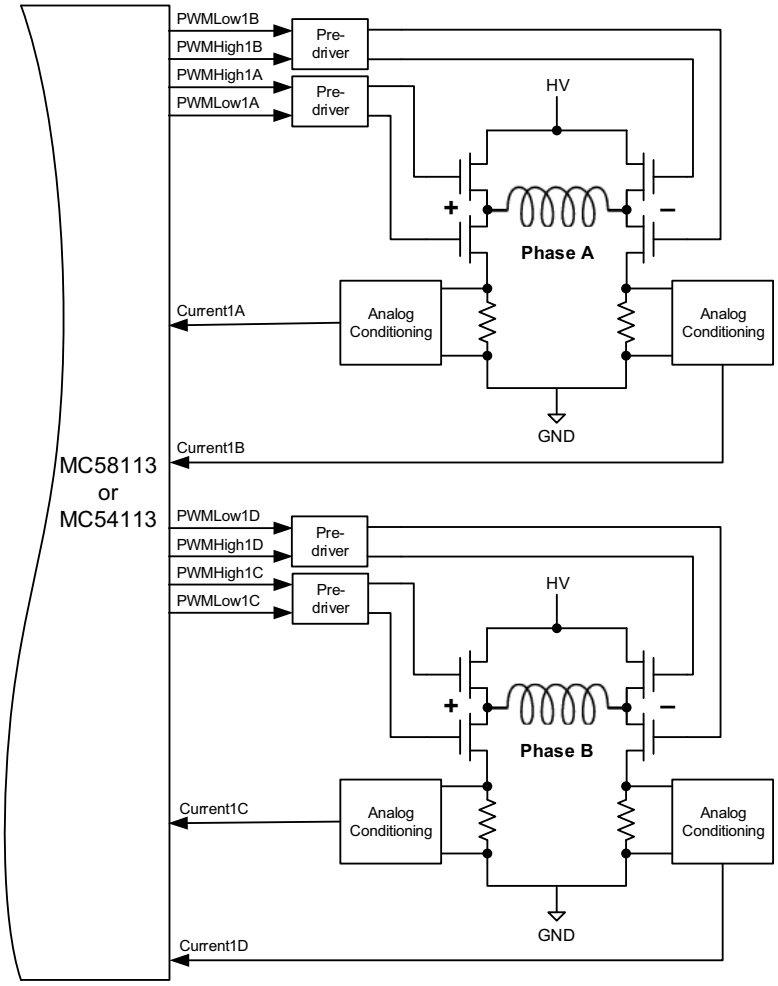


Figure 6-4: Two-phase Step Motor Bridge Configuration

6.2.3.1 Step Motor Amplifier Connections

As shown in the table below eight PWM output signals and four analog feedback signals interface between the MC58113 IC and the switching amplifier circuitry.

MC58113 signal	Description
PWMHigh1A	Digital high side drive output for motor phase A, positive coil terminal
PWMLow1A	Digital low side drive output for motor phase A, positive coil terminal
PWMHigh1B	Digital high side drive output for motor phase A, negative coil terminal
PWMLow1B	Digital low side drive output for motor phase A, negative coil terminal
PWMHigh1C	Digital high side drive output for motor phase B, positive coil terminal
PWMLow1C	Digital low side drive output for motor phase B, positive coil terminal
PWMHigh1D	Digital high side drive output for motor phase B, negative coil terminal
PWMLow1D	Digital low side drive output for motor phase B, negative coil terminal
Current1A	Analog input containing the current flow through the positive leg of the phase A bridge
Current1B	Analog input containing the current flow through the negative leg of the phase A bridge
Current1C	Analog input containing the current flow through the positive leg of the phase B bridge
Current1D	Analog input containing the current flow through the negative leg of the phase B bridge

6.2.4 Amplifier-Related Parameters

There are a number of MC58113 IC parameters which are used to set or control the switching amplifier and related current sense circuitry shown in Figures 6-2 through 6-4.

The following table shows these various amplifier-related settings.

Parameter	Range & Units	Description
Motor Output Mode	PWM High/Low 50/50 PWM Sign/magnitude PWM SPI DAC-Offset SPI DAC-two's complement Pulse & Direction SPI Atlas	PWM High/Low mode or 50/50 PWM mode must be used for operation when the MC58113's current control is active. For non-current control operation any of the PWM modes may be selected. To generate an analog motor command signal the SPI DAC modes are used. Pulse & Direction is selected for use with a step motor amplifier supporting those input signals. SPI Atlas specifies that an Atlas Digital amplifier will be used. This parameter is set using the **SetOutputMode** command.
PWM Switching Frequency	20 KHz 40 KHz 80 KHz	Higher inductance motors should be set for 20 kHz. Lower inductance motors may use 40 or 80 kHz to maximize current control accuracy and minimize heat generation. This parameter is set using the **SetDrivePWM** command. The default value for this parameter is 20 kHz.
PWM Dead Time	0-16,383 nSec	The correct setting of this parameter depends on the specific switching circuitry used. See the manufacturer's data sheet for more information. This parameter is set using the **SetDrivePWM** command, and has units of nSecs.
Analog Current Offset A-D	-32,767 to 32,768 counts	The analog offset 'zero offset values' are determined when the amplifier is switching with a zero current command. The offsets are generally specific to the external circuitry of each leg current sensor, and should be separately zeroed out for best performance. These parameters are set using the **SetAnalogCalibration** command or via the **CalibrateAnalog** command.
PWM Refresh Time	0-32,767 nSec	Some high-side switch drive circuitry requires a minimum amount of off time, applied at a programmable period interval, to allow the charge pump circuitry to refresh. The PWM Refresh Time parameter, set using the **SetDrivePWM** command, specifies this refresh time and has units of nSecs.
PWM Refresh Period	1-32,767 cycles	Some high-side switch drive circuitry requires a minimum amount of off time, applied at a programmable period interval, to allow the charge pump circuitry to refresh. The PWM Refresh Period parameter, set using the **SetDrivePWM** command, specifies this refresh time period and has units of current loop cycles.
Minimum Current Read Time	0-16,383 nSec	When using Brushless DC motors if two of three legs are driven at 100% the analog current reading of the second leg low-side switch needs to be active for a minimum amount of time for a valid current reading. This parameter, set using the **SetDrivePWM** command, specifies the amount of time needed for a valid analog current read when the drive is in this condition. This parameter has units of nSecs.

6.2.5 Amplifier and Current Control-Related Circuitry

Both discrete components and integrated bridge ICs or modules may be used for the bridge electronics with current control active. Depending on the switch control interface 50/50 PWM mode or PWM High/Low should be selected.

Current sensors consist of sense resistors, as shown in Figures 6-2 through 6-4, or linear Hall sensors. The analog processing circuitry required for each is somewhat different. If sense resistors are used ground-referenced operational amplifiers may be used.

Current inputs are sampled by the MC58113 at a rate of 20 kHz and should be filtered to minimize noise. A low pass filter with a rolloff of 200 kHz - 1,000 kHz is recommended, with 500 kHz being a typical value for most applications. MC58113s operating at 20 kHz PWM frequency in high noise environments may consider a rolloff on the lower end of the frequency range. MC58113s with PWM frequencies of 40 kHz or 80 kHz operating in low or normal noise enviroments may consider a rolloff on the higher end of this range.

See Section 7.12, "PWM High/Low Motor Drive With Leg Current Sensing/Control," for example schematics for various MC58113-based amplifier designs with current control.

6.2.6 Current Scaling, Reading and Writing

The value of the sense resistors and downstream analog conditioning circuitry shown in Figures 6-2 through 6-4 determine the overall controllable current range of the switching amplifier. The overall current sense range should be 25% to 50% above the largest expected peak current. The commandable current range is 80% of the total current sense range.

Assuming that an analog voltage reference range of 3.30 volts is used (set via the *AnalogRefHigh* and *AnalogRefLow* pins), the total current range is represented by a bi-polar voltage centered around 1.65V at the *CurrentIA-D* input pins. In this scheme zero volts represents the largest possible negative current and +3.30V represents the largest possible positive current.

Example: A Brushless DC motor application will allow a peak current in each phase of 7.5 amps. The total current sense is selected as +/- 10.0 amps, which gives a commandable range of +/- 8.0 amps. A sense resistor and op amp are used to generate +/- 1.65 volts for the desired current range of +/- 10 amps giving a current scaling of 10.0 amps/ 1.65 volts or 6.06 amps/volt.

Motor currents are read using the **GetCurrentLoopValue** or **GetFOCValue** command. The returned value is a signed twos-complement number with a full scale negative current value of -20,479, a zero current value of 0, and full scale positive value of 20,479. This same scaling is used to set as well as read quantities that represent motor currents.

Example: In the above system, the scaling of measured current to current in counts is 10.0 amps / 20,479 counts = .488 mA/count. To set an I^2t continuous current of 3.5 amps a value of 3,500 mA / .488 mA/count = 7,172 counts is used.

6.2.7 Minimum Current Read Time

When controlling Brushless DC motors with FOC (field oriented control) current control mode selected the MC58113's minimum current read time parameter is used to insure a valid leg current reading when two of the three phases have a saturated PWM signal. This period of time is affected by the analog processing circuitry. It can be approximated by taking the electrical time constant and multiplying by 3 to 5.

6.2.8 Leg Current Analog Input Offsets

To improve efficiency and motion smoothness it is important that the leg current inputs on signals *Current I A-D* represent the actual absolute current value as accurately as possible.

To facilitate this the MC58113 provides the ability to zero-out analog input offsets that may exist while the motor coils are not being driven by the amplifier and the motor is not moving.

The simplest way to do this is to send a **CalibrateAnalog** command to the MC58113. This command will automatically measure and set the offsets so that the leg current analog inputs are zeroed out. Because a number of samples are taken and averaged, 100 mSec should be allowed for this command to complete. In addition, current loop should be disabled and the motor command set to zero before this command is executed.

Alternatively, it is possible to directly read each analog input via the **GetAnalog** command and then write the same values for the corresponding analog offsets using the **SetAnalogCalibration** command. When using this manual method it is recommended that a number of analog reads of each signal are averaged together to improve the offset accuracy.

Regardless of the motor type (Brushless DC, DC Brush, step motor) having correctly calibrated offsets of the analog leg current inputs is important to maximize motor drive efficiency and smoothness. Failure to calibrate these analog offsets may result in reduced drive efficiency and uneven motion.

6.2.9 Other Amplifier Related Signals

6.2.9.1 AmplifierEnable Signal

The MC58113 provides a hardware signal output that indicates whether the external amplifier circuitry should be active or not. While not all external amplifiers will require or provide such an input control, this signal is useful for general safety purposes, as well as to simplify the task of insuring a startup without jogging the motor after powerup.

The output of this signal corresponds directly to the state of the motor output bit of the active operating mode register. If this bit is on, the *AmplifierEnable* signal is active, and vice versa.

6.2.9.2 PWMOutputDisable Signal

The MC58113 inputs a high speed PWM output disable that may be useful for safety protection when the motor output mode is set to PWM High/Low or Sign/Magnitude PWM. When the input is driven active PWM output is driven to a disabled state. PWM operation is normal when this signal is inactive.

The most common use of this signal is for very high speed shutdown of the amplifier circuitry if an external condition is detected that may damage the amplifier or related drive circuitry.

6.3 Overtemperature Protection

MC58113 supports a temperature sensor input at the *Temperature* pin to continuously monitor the temperature of the power electronics or another part of the drive.

6.3.1 Overtemperature-Related Circuitry

Although various temperature sensors may be used with the MC58113, the most common type of sensor is a thermistor.

When using a thermistor the *Temperature* input signal should be filtered to minimize noise. The *Temperature* input is sampled by the MC58113 at a rate of 1kHz or higher, and therefore a low pass filter with a rolloff at 500 Hz or lower is recommended.

See Section 7.10, "Drive-Related Safety and Monitoring Features ," for an example schematic of temperature input using the MC58113.

6.3.2 Overtemperature Scaling, Reading and Writing

The value of the temperature sensor and downstream analog conditioning circuitry determine the overall remperature range that can be measured. The overall temperature sense range should be 15% to 25% above the highest expected temperature.

The *Temperature* signal input expects a voltage in the range of 0V to 3.3V (unless otherwise set via the *AnalogRefHigh* and *AnalogRefLow* signals) representing the sensed temperature. Both temperature-voltage-increasing (voltage increases with increasing temperature) and temperature-voltage-decreasing (voltage decreases with increasing temperature) thermistors are supported. For voltage increasing thermistors 0.0V represents the lowest possible temperature, and for voltage decreasing thermistors 3.3V represents the lowest possible temperature.

When reading the temperature via the MC58113's **GetDriveValue** command or via a trace the returned value is an unsigned number with a range from 0 to 32,767. The returned temperature is direction adjusted, meaning for both voltage-increasing and voltage-decreasing thermistors a zero return value indicates the lowest possible temperature and a 32,767 represents the highest possible temperature.

Example: A temperature-voltage-increasing thermistor and associated analog processing circuitry generate a voltage of 2.9V when the switching bridge circuitry is at the hottest safely operable temperature. The overtemperature limit specified using the **SetDriveFaultParameter** command should thus be set to 32,768 * 2.9V/3.3V = 28,796.

The overtemperature functions continuously once programmed. To disable the overtemperature check a threshold value of 32,767 is set.

Converting MC58113-readable values to an actual temperature in units of degrees C is often complex. For this reason the MC58113's overtemperature protection mechanism compares directly against the unconverted temperature value in units of counts, not units of degrees C.

6.4 DC Bus Management

Figure 6-5: DC Bus Monitoring Circuitry

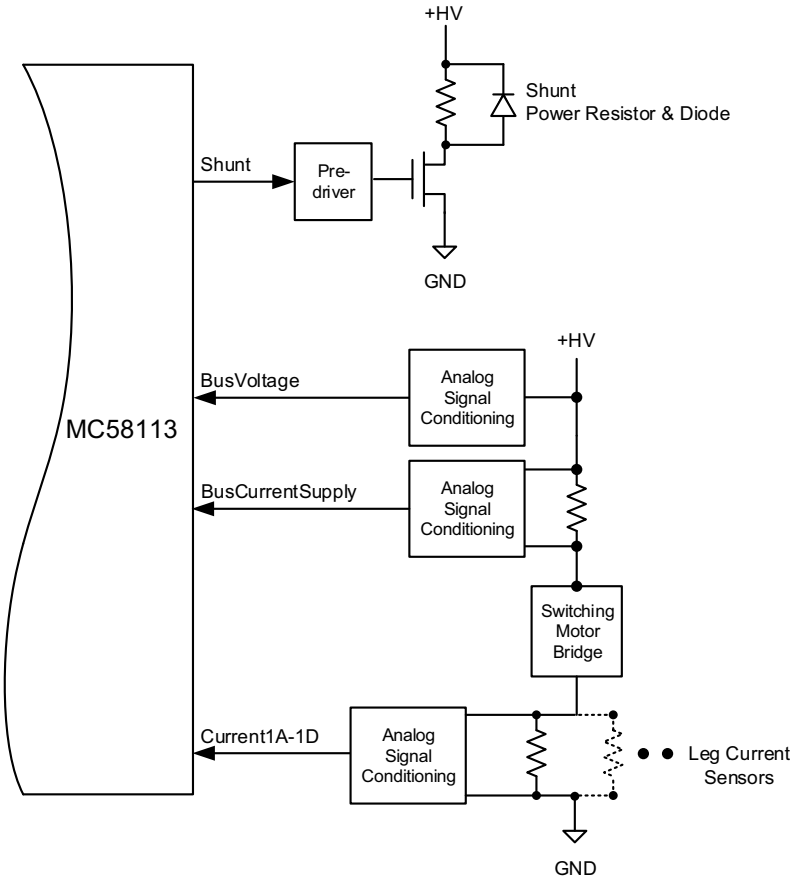


Figure 6-5 shows the DC bus monitoring scheme used with the MC58113 IC. The provided safety functions include over current protection, over and under voltage detection, and shunt resistor control.

6.4.1 DC Bus Overcurrent Monitoring

DK58113 monitors both the supply-side and return-side DC bus current to detect overcurrent conditions.

6.4.1.1 DC Bus Overcurrent-Related Circuitry

The *BusCurrentSupply* signal encodes the total current flowing through the motor amplifier bridge(s) from the +HV supply.

The DC bus current supply sensor typically consists of a sense resistor, as shown in Figure 6-5, or a linear Hall sensor. The analog processing circuitry required for each is somewhat different. If a dropping resistor is used an isolating operational amplifier, current mirror, or similar circuit should be used. Linear Hall sensors typically use just a ground-referenced operational amplifier.

The *BusCurrentSupply* feedback signal should be filtered to minimize noise, and the source impedance of the signal conditioning circuit should be less that 100 ohms. A peak holding circuit is recommended with a hold time of 100 µSec. Current inputs are sampled by a dedicated high speed circuit internal to the MC58113. To minimize false positives a low pass filter with a rolloff of 200 kHz - 500 kHz is recommended with a typical value of 350 kHz.

See Section 7.10, "Drive-Related Safety and Monitoring Features ," for example schematics of a typical MC58113-based DC bus management designs.

During motor braking or other motion conditions it may be possible for the DC bus supply current flow to be negative. Care should be taken to insure that negative currents do not generate a negative voltage at the MC58113's BusCurrentSupply analog input pin. This is generally accomplished via a diode. See Section 7.10, "Drive-Related Safety and Monitoring Features ," for examples of DC bus safety-related schematics.

6.4.1.2 DC Bus Supply Current Scaling, Reading and Writing

The value of the sense resistor and downstream analog conditioning circuitry determine the overall current range that can be measured. For the DC bus supply current input this range should be approximately double the maximum expected DC bus peak current flow. Note that in the case of step motors the maximum DC bus current is 150% of the peak phase current.

The *BusCurrentSupply* input range is 0.0V to 3.30V (if *AnalogRefHigh* and *AnalogRefLow* are set accordingly), with 0.0V representing no (zero) current flowing and 3.3 volts representing the maximum measurable amount of current flowing.

Example: A DC bus overcurrent function is being designed for a Brushless DC motor with maximum peak current of 5.0 amps. In this application a sense resistor and op-amp set the current measurement range at 0 to 10.0 amps.

The measured bus supply current can be read using the **GetDriveValue** command. The returned value is an unsigned 16-bit number with range of 0 to 65,535. The DC bus supply overcurrent threshold is set using the **SetDriveFaultParameter** command. Typical threshold settings are 75-95% of the current sense range.

Example: An isolating op-amp and sense resistor generate 3.3V at a DC bus supply current flow of 15 amps. The scaling of current reads is 15.0A/65,536 = .228 mA/count. The overcurrent threshold is set at 12.0 amps, or 12,000 mA/.228 mA/count = 52,631.

The DC Bus supply overcurrent threshold function operates continuously once programmed. To disable an overcurrent check a threshold value of 65,535 is set.

6.4.1.3 DC Bus Return Current Scaling, Reading and Writing

Return current flow from the DC bus is measured via the leg current sensors as part of the current control mechanism. See Section 6.2.6, "Current Scaling, Reading and Writing," for more information on leg current scaling.

The bus return current can be read using the **GetDriveValue** command. The returned value is an unsigned 16-bit number with range of 0 to 20,479. The DC bus return overcurrent threshold is set using the **SetDriveFaultParameter** command.

The DC Bus return overcurrent threshold function operates continuously once programmed. To disable an overcurrent check a threshold value of 32,767 is set.

If current control is not implemented then it is not possible for the MC58113 to measure DC bus return current.

6.4.2 DC Bus Voltage Monitoring

The MC58113 can monitor the DC bus voltage for overvoltage and undervoltage conditions utilizing the *BusVoltage* analog input signal. Overvoltage and undervoltage detection is accomplished by checking the measured voltage of the DC bus and comparing with user-provided thresholds.

6.4.2.1 DC Bus Voltage-Related Circuitry

The DC bus voltage sensor typically consists of a voltage divider, as shown in Figure 6-5. The analog processing circuitry required for each is somewhat different. If a resistor is used an isolating operational amplifier, current mirror, or similar circuit should be used.

The *BusVoltage* signal should be filtered to minimize noise. The DC bus voltage input is sampled by the MC58113 at a rate of 20kHz, and therefore a low pass filter with a rolloff of 10 kHz or less is recommended.

See Section 7.10, "Drive-Related Safety and Monitoring Features ," for example schematics of typical MC58113-based DC bus management designs.

6.4.2.2 DC Bus Voltage Scaling, Reading and Writing

The value of the sense resistor and downstream analog conditioning circuitry determines the overall voltage measurement range. This overall voltage range should be 15% to 50% above the maximum expected DC bus voltage.

The *BusVoltage* input range is 0.0V to 3.30V, with 0.0V representing a DC bus voltage of 0V, and +3.3V representing the largest measurable DC bus voltage. The measured bus voltage current can be read using the **GetDriveValue** command. The returned value is an unsigned 16-bit number with range of 0 to 65,535. The over and undervoltage thresholds are set using the **SetDriveFaultParameter** command, and have the same units.

Example: In an application that will have a motor voltage of 48 volts, external circuitry has been selected to present 3.3V at the BusVoltage input when the DC bus voltage is 65 volts. The scaling is 65V/65,536 or .992 mV/count. To set an undervoltage threshold of 45V a value of 45,000 mV/.992 mV/count = 45,362 is specified. To set an overvoltage threshold of 52V a value of 52,000 mV/.992 mV/count = 52,419 is specified.

The under and overvoltage thresholds function continuously. To disable the under voltage or over voltage check, threshold values are set to 0 or 65,535 respectively.

6.4.3 Shunt Resistor

As shown in Figure 6-5 the MC58113 controls a shunt PWM output, which in turn typically drives a MOSFET or IGBT switch which connects the voltage to the DC bus ground via a power resistor, thereby lowering the DC bus voltage.

The shunt functions by continually comparing the DC bus voltage, as presented at the *BusVoltage* signal, to a user programmable threshold. If the DC bus voltage exceeds the comparison threshold the *Shunt* signal outputs a PWM waveform at a user programmable duty cycle. This PWM frequency is equal to the motor drive PWM frequency. Once active, shunt PWM output will stop when the DC bus drops to 2.5% below the threshold comparison value.

Once programmed, the shunt comparison function operates continuously. To disable it, a value of 32,767 should be programmed. The shunt function is not active when motor output is not enabled (the active operating mode output bit is not set).

6.4.3.1 Shunt Related Circuitry

The shunt resistor connected should have a resistance such that the current flow through the shunt switch, diode and resistor do not exceed the ratings of those components at the expected DC bus voltage. The diode, which is connected in parallel to the resistor, should have a voltage and current rating at least equal to those of the switch. See Figure 7-9 for more information.

6.4.3.2 Shunt Reading and Writing

To set the shunt DC bus voltage comparison threshold the **SetDriveFaultParameter** is used. The scaling and units are the same as for the over and undervoltage functions. The shunt PWM duty cycle is set using the

SetDriveFaultParameter command, and the provided value is an unsigned 16-bit number with range of 0 to 32,767.

Example: In the system from the example in Section 6.4.2.2, "DC Bus Voltage Scaling, Reading and Writing," the shunt will be activated when the DC bus voltage climbs to 51 volts with a duty cycle of 95%. The shunt comparison threshold is set to 51,000 mV/1.98 mV/count = 25,757 and the duty cycle value is .95 * 32,768 = 31,130.

It is possible to determine whether the shunt output is active at any given moment. To do this the command **GetDriveStatus** is used and bit #4 of the returned status word should be checked.

6.5 Analog Input Signals

The MC58113 provides a number of direct analog input signals in connection with current control, DC bus voltage monitoring, temperature monitoring, and overcurrent monitoring functions. For information on how these various analog signals are used refer to the corresponding sections of this manual that describe those functions.

In addition to the above current control and safety-related analog inputs the MC58113 provides a signal, *AnalogI*, that serves as a general purpose user-defined analog input. As for all analog input signals the allowed signal input range is *AnalogRefLow* to *AnalogRefHigh*. If unused, *AnalogI* should be connected to *AnalogGND*. Refer to Section 5.5, "MC58113-Series ICs Pin Descriptions," for more details.

For additional information on the *AnalogI* signal along with a complete example schematic see Section 7.9, "General Purpose Analog Input."

6.5.1 Reading Analog Signal Input Values

To directly read the value of the analog inputs the command **ReadAnalog** is used. There are eight inputs each with a unique PortID that is specified when using this command. The table below shows the PortID values for each analog input signal.

Signal Name	Pin #	PortID
AnalogI	21	0
CurrentIA	23	1
CurrentIB	28	2
CurrentIC	22	3
CurrentID	29	4
Temperature	31	5
BusCurrentSupply	19	6
BusVoltage	20	7

For information on the format and scaling of values returned by this command refer to the *C-Motion Magellan Programming Reference*.

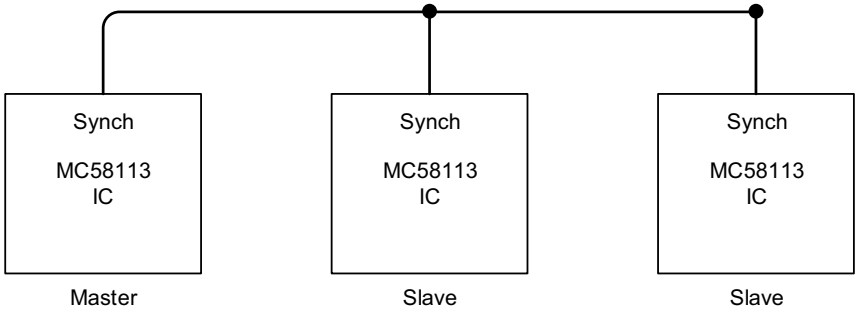
6.6 Multi-chip Synchronization

The MC58113 supports the ability to explicitly synchronize profile and servo updates across multiple MC58113 chips or to separate external synch sources.

To connect two or more MC58113s for synchronization a connection of the *Synch* pins is required. For more information on synchronizing multiple MC58113s, see the *Magellan Motion Control IC User Guide*.

The following diagram shows three synchronized MC58113s.

Figure 6-6: Synch Signal Connections



6.7 MC58113 Memory Buffers

Figure 6-7: MC58113 Memory Buffers

Start Address (in Hexadecimal)	Function
0x0000 0000	Trace RAM (16,380 words)
0x0000 3FFC	Reserved
0x2000 0000	NVRAM reserved header (4 words)
0x2000 0004	NVRAM programmable header (4 words)
0x2000 0008	NVRAM initialization (1,016 words)
0x2000 0400	Reserved

MC58113 provides the ability to store and retrieve buffer data internally. There is a general purpose RAM, and an area that is used to store non-volatile initialization commands. Figure 6-7 shows this internal memory space.

Although MC58113 allows up to 32 different buffers to be defined, typically, there will just be two buffers, the general purpose trace RAM area, and the NVRAM area. For convenience these buffers are predefined in the MC58113 as buffer #0, and buffer #1 respectively.

Figure 6-7 shows the MC58113's memory space in 16-bit word addressing. However because trace functions use 32-bit word addressing, when setting up trace buffers the address should be divided by two.

For more information on Magellan IC memory buffers and trace, see the *Magellan Motion Control IC User Guide*.

6.7.1 MC58113 Non-Volatile Storage

As shown in Figure 6-7, MC58113 supports a 1,024 word memory segment that is non-volatile (NVRAM). The primary purpose of the NVRAM is to allow MC58113 configuration information to be stored, so that upon power up it can be loaded automatically rather than requiring an external controller to perform this configuration initialization function.

If non-volatile initialization commands have been loaded the power-up sequence detects this and begins processing it. Note that processing stored initialization commands may increase the overall initialization time of the MC58113 depending on the sequence stored.

The order of initialization for most commands does not matter. However there are some restrictions; **SetMotorType** should be the first executed command, and commands that enable MC58113 for operation such as **SetOperatingMode**, **Update**, and **SetOutputMode** should be last.

Initialization commands in the NVRAM storage that result in axis motion are not recommended. While not specifically disallowed it is recommended that the host send these commands after NVRAM initialization is completed.

If there are errors in the stored sequence then an instruction error code will be loaded so that the error can later be diagnosed. MC58113 will abort initialization if it detects any error while processing commands. If an error is detected the host controller can send a **GetInstructionError** to diagnose the nature of the erroneous command processed during initialization.

6.7.1.1 NVRAM Format

Addresses 0x2000 0000 through 0x2000 0003 hold a reserved four-word block that must have a value of 0.

Addresses 0x2000 0004 through 0x2000 0007 hold a four-word user-programmable header block that may hold any stored information useful for the user application.

Initialization commands are stored beginning at address 0x2000 0008. MC58113 parameter data stored into NVRAM for initialization is similar, but not identical to SPI host communication formatting. The first word of each command entry represents a header which should have 00 in the high byte, and in the low byte the logical negation of an 8-bit ones complement checksum computed over all bits in the command packet except for the checksum field and a seed of 0xAA. The subsequent words represent the command packet data, the format of which is detailed in the *C-Motion Magellan Programming Reference*.

Example: The table below shows an example initialization sequence. Word addresses are given as offsets from the NVRAM initialization command address of 0x2000 0000.

NVRAM Word Address	Mnemonic	Stored Word(s)	Comments
+0 - +3		0, 0, 0, 0	Four words of reserved header must be set to zero
+4 - +7	"CONFIG 1"	0x434F, 0x4E46, 0x4947, 0x2031	Header may contain anything, but in this example contains ASCII encoding of "CONFIG 1" string
+8	SetFOC D KpDQ 0x1234	0x0018	checksum in low byte
+9		0x00F6	axis # 1 (0), SetFOC opcode (0xF6)
+0xA		0x0000	argument 1: D (Direct), KpDQ
+0xB		0x1234	argument 2: 0x1234 value
+0xC	SetFOC D KiDQ 0x5678	0x008E	checksum in low byte
+0xD		0x00F6	axis # 1 (0), SetFOC opcode (0xF6)
+0xE		0x0001	argument 1: D (Direct), KiDQ
+0x0F		0x5678	argument 2: 0x5678 value
+0x10	Update	0x003B	checksum in low byte
+0x11		0x001A	axis # 1 (0), Update opcode (0x1A)
+0x12	SetOperatingMode 7	0x00E8	checksum in low byte
+0x13		0x0065	axis # 1 (0), SetOperatingMode opcode (0x65)
+0x14		0x0007	argument 1: enable output, current loop on

MC58113 allows general purpose application information to be stored at the end of the initialization command sequence. To separate this user application information from the initialization command sequence a separator consisting of four consecutive 0xffff words is used at the end of the command sequence.

In the example above, this would mean 0xffffs are stored at +0x15 - 0x18, with the user-specific general purpose NVRAM data starting at +0x19.

6.7.1.2 Storing to NVRAM

The following sequence is used to store command initialization data or other data to the MC58113 non-volatile memory area:

1. Send a **NVRAM** command with an argument of *NVRAMMode*. Sending this command places MC58113 in a special mode allowing it to store memory into the NVRAM. Before proceeding the external controller should delay 1 second or more.
2. Send a **NVRAM** command with an argument of *EraseNVRAM*. This command will erase the entire NVRAM memory area. Before proceeding the external controller should delay four seconds or more.
3. For each 16-bit word of data that is to be written into the NVRAM area the command **NVRAM** with an argument of *Write* is sent, along with the data word to be written. The first word is written to address 0x2000 0000. After each word is written MC58113 increments an internal pointer so that subsequent data words are automatically stored in the correct location.
4. Once all data is successfully written the external controller should send a **Reset** command, which will cause MC58113 to reboot and execute a power up sequence. Note that this power-up sequence will include processing the stored data sent using the above sequence.

6.7.1.3 Reading from NVRAM

It is possible to directly read the MC58113 NVRAM memory area using buffer commands. See the table at the beginning of Section 7.3, "Power Supplies," for more information on MC58113 buffer processing.

6.8 Output Signal Status During Powerup

The following table summarizes the MC58113's output signal states during power up and after powerup when no initialization data is stored in the MC58113's NVRAM.

Pin Name	Pin #	State During Powerup	State After Powerup
PWMHighIA/PWMMagIA	87	tri-stated	tri-stated
PWMLowIA/PWMSignIA	86	tri-stated	tri-stated
PWMHighIB/PWMMagIB/PulseI	84	tri-stated	tri-stated
PWMLowIB/DirectionI	83	tri-stated	tri-stated
PWMHighIC/PWMSignIB/AtRestI	82	tri-stated	tri-stated
PWMLowIC	76	tri-stated	tri-stated
PWMHighID	74	tri-stated	tri-stated
PWMLowID	73	tri-stated	tri-stated
AmplifierEnableI	54	tri-stated	driven low (inactive)

Pin Name	Pin #	State During Powerup	State After Powerup
Shunt	8	tri-stated	tri-stated
AxisOut1	65	pulled high	driven high (active)
FaultOut	57	tri-stated	driven low (inactive)
SrlXmt	43	pulled high	pulled high
CANXmt	40	tri-stated	pulled high
SrlEnable/HostSPIStatus	9	tri-stated	driven low (inactive)
AmplifierSPIClock	85	pulled high	pulled high
AmplifierSPIXmt	10	tri-stated	tri-stated
~AmplifierSPIEnable	89	pulled high	pulled high
HostSPIXmt	95	pulled high	pulled high
~HostInterrupt	66	pulled high	driven high (inactive)
Synch	58	tri-stated	pulled high

If configuration data has been stored in the MC58113's NVRAM then the final powerup condition of various outputs signals may be affected. See the detailed description of the specific commands that are stored into the NVRAM for details.

For more information on NVRAM initialization storage see Section 6.7.1, "MC58113 Non-Volatile Storage."

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7. Application Notes — MC58113

7

In This Chapter

- General Design Notes
- Design Tips
- Power Supplies
- Clock Generator, Grounding and Decoupling, and Device Reset
- Reset Signal
- Serial Communication Interface (SCI)
- CAN Communication Interface
- Host SPI Communication Interface
- General Purpose Analog Input
- Drive-Related Safety and Monitoring Features
- Shunt Resistor Drive
- PWM High/Low Motor Drive With Leg Current Sensing/Control
- Dual DC Brush Motor Control Using Atlas Digital Amplifier
- DC Brush Motor Control Using SPI Interfaced DACs
- DC Brush, Brushless DC and Step Motor Drive using PWM Output
- Using the Allegro A3977 to Drive Microstepping Motors

7.1 General Design Notes

Logic functions presented in the example schematics are implemented by standard logic gates. In cases where specific parameters are of significance (propagation delay, voltage levels, etc.) a recommended part number is given.

In the schematics, pins with multiple functions are referenced by the name corresponding to the specified functionality. For example, pin 87 on the MC58113 is named "PWMHigh1A/PWMMag1A/Pulse1" but will be referenced by the name "PWMHigh1A" in the PWM High/Low motor drive example and "PWMMag1A" in the DC brush motor schematics.

The schematic designs presented in this chapter are accurate to the best of PMD's knowledge. They are intended for reference only and have not all been tested in hardware implementations.

7.1.1 Interfacing to Other Logic Families

When integrating different logic families, consideration should be given to timing, logic level compatibility, and output drive capabilities. The MC58113 is 3.3V CMOS input/output compatible and cannot be directly interfaced to 5V CMOS components. In order to drive a 5V CMOS device, level shifters from the 5V CMOS AHCT (or the slower HCT) families can be used. When using a 5V CMOS component to drive the CP, a voltage divider may be used or a member from the CMOS 3.3V LVT family may serve as a level shifter.

7.2 Design Tips

7.2.1 Controlling PWM Output During Reset

When the MC58113 is in a reset state (when the reset line is held low), or immediately after a power on, PWM output will be in a high impedance state, which will provide design flexibility to prevent undesirable motor movement at system level. For example, when the power train is active high in PWM High/Low mode, pull-down resistors can be used to keep the power train off during reset and power up. For an active low power stage, pull-up resistors can be used.

7.2.2 Using a Non-Standard System Clock Frequency

It is often desirable to share a common clock among several components in a design. In the case of the MC58113 IC it is possible to use a clock below the standard value of 10 MHz. In this case, all system frequencies will be reduced as a fraction of the input clock versus the standard 10 MHz clock. The following list details the affected system parameters.

- Serial baud rate
- PWM carrier frequency, deadtime, refresh time, current sense time
- Cycle time
- Commutation and current loop rate
- Encoder-related timing
- HostSPI-related timing
- AmplifierSPI-related timing

For example, if an input clock of 8 MHz is used with a serial baud rate of 9600, here are example timing changes that will result.

- Serial baud rate decreases to 9600 bps *8/10 = 7680 bps
- PWM frequency decreases to 20 kHz *8/10 = 16 kHz
- Total cycle time increases by a factor of 10/8
- The commutation rate for brushless axes decreases to 10 kHz *8/10 = 8 kHz

7.2.3 Thermal Considerations

The recommended operating junction temperature range for the MC58113 is between -40°C and 105°C. Proper thermal design will ensure the system reliability. Based on a simplified resistor model for heat transfer, following thermal matrices under different conditions are provide to for thermal design.

	AIR FLOW			
Parameter	**0 lfm**	**150 lfm**	**250 lfm**	**500 lfm**
θ_{JA}[°C/W] High k PCB	42.2	32.4	30.9	28.7
ψ_{JT} [0°C/W]	0.4	0.6	0.7	0.9

θ_{JA} is the junction-to-ambient thermal resistance. Although it is an important design reference, this thermal metric highly depends on the board design and system configurations. Directly using it for junction temperature estimation could result in misleading results because the environmental factors are different from design to design.

ψ_{jT} (junction to top of package) is provides as an useful thermal matric for estimating the in-situ junctional temperature. The environmental factors do not affect this metric as much, and it can be easily measured. Also, because ψ_{jT} is small, if a user chooses to, the top of package temperature might be approximated as the junctional temperature for design estimation when enough thermal design margin is included.

7.3 Power Supplies

In the schematic shown in Figure 7-1 the design is powered by an external +5VCC power source. The MC58113 requires a 3.3V supply input. +3.3V, the 3.3V digital supply, is generated by the TPS76733QPWPRG4, a 1.0 Amp fixed 3.3V low-dropout voltage regulator.

If the MC58113 analog-to-digital converter (ADC) is used it should be supplied with a filtered +3.3Vs supply.

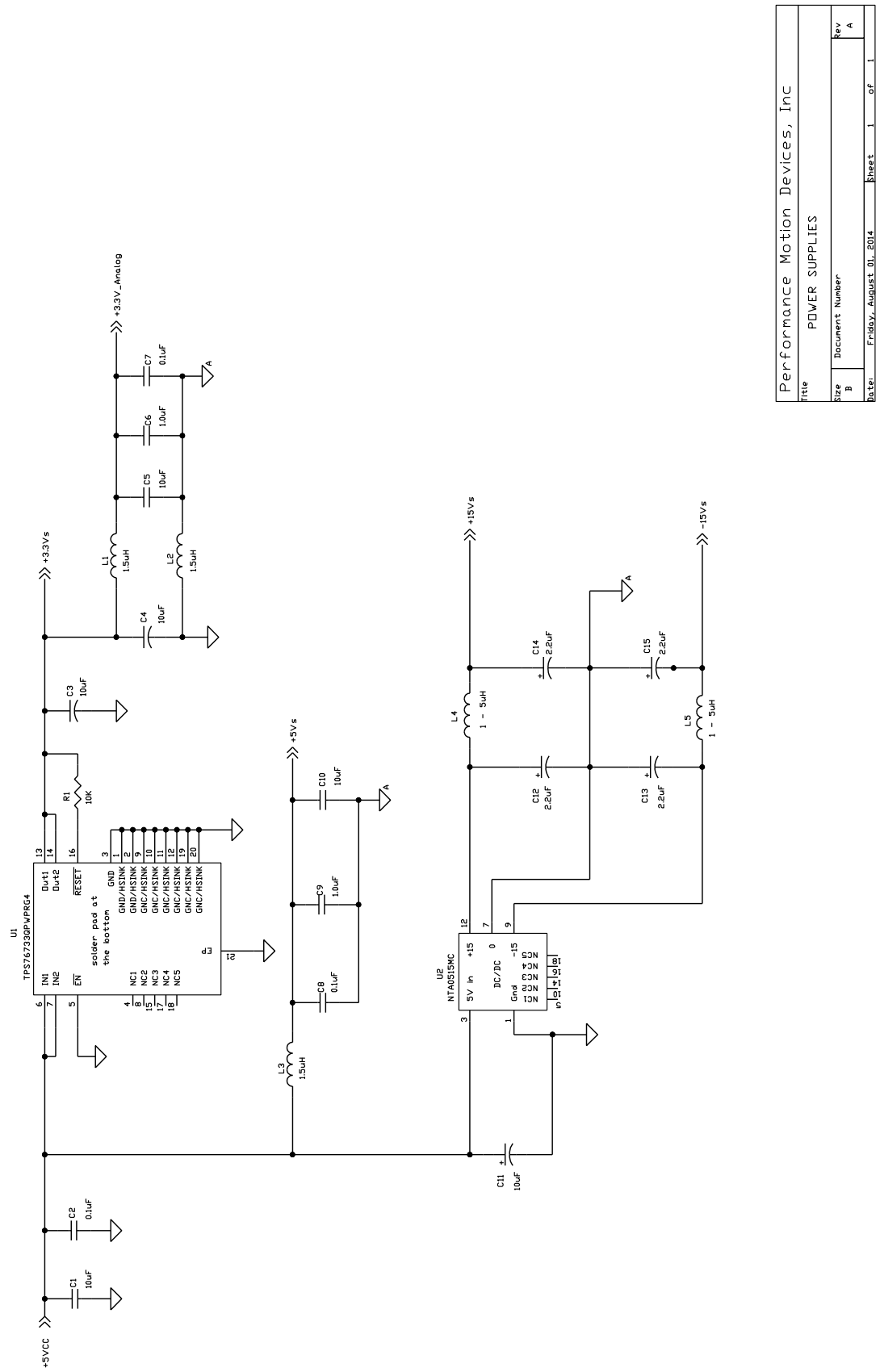
The following is the list of supplies which are referenced in the example schematics within this application notes section of the manual:

- +3.3Vs and +3.3V_Analog: +3.3Vs is the main digital supply for the MC58113 device. +3.3V_Analog is the filtered version of the +3.3Vs supply for ADC and its related conditioning circuitry. The extra filtering is used to provide additional decoupling of the analog elements from the digital elements in the circuitry.
- +5Vs: is a filtered version of +5VCC used for analog components requiring +5V supplies. The extra filtering is used to reduce the voltage ripple and to generate additional decoupling of the analog elements from the digital elements in the circuitry.
- ±15Vs: ±15V supplies: is used for analog components such as MOSFET gate drivers and SPI DACs. The Murata NTA0515MC is a 1W ±15V DC/DC converter which delivers ±33 mA. Depending on the current load of the final design, a different power capacity DC/DC converter may be required. An LC filter is used to reduce the voltage ripple.

Notes:

- The power supplies schematic provided in Figure 7-1 is for reference only, and is designed only to meet the requirements of the example schematics used in the application notes section of the manual. The actual supplies used should be designed according to the stability and precision requirements of the application.
- Power supplies for the motor drive amplifiers/switchers are not shown. Care should be taken when designing these power supplies, as they should be capable of sinking high switching currents.

Figure 7-1: Basics, Power Supplies, 58113



7.4 Clock Generator, Grounding and Decoupling, and Device Reset

7.4.1 Clock Generator — MC58113

An external 3.3V 10MHz clock oscillator output should be supplied to the MC58113's ClkIn pin.

7.4.2 Grounding and Decoupling

As shown in Figure 7-2, each of the MC58113 digital supply voltage pins should be connected to the +3.3 Vcc. A minimum of 1.2 µF capacitor should be used to decouple each Vcc pin. A 2.2 µF ceramic capacitor is recommended. If the +3.3 Vcc source is noisy, additional ferrite bead can be placed in series with the decoupling cap to form a LC filtering network on the power pin.

Each of the "FltCap" pins should be connected to a minimum of 1.2 µF filtering capacitor which in turn connects to ground. A 2.2 µF ceramic capacitor is used in the schematic. The filtering capacitors must be placed as close as possible to each one of the "FltCap" pins. This general rule applies to all analog and digital components, although in some of the schematics that follow these capacitors are not shown for reasons of brevity. In some cases, especially for analog processing circuitry, it may be beneficial to run a separate power line from the power supply to the component in order to prevent power supply fluctuations from impacting low-level signal components.

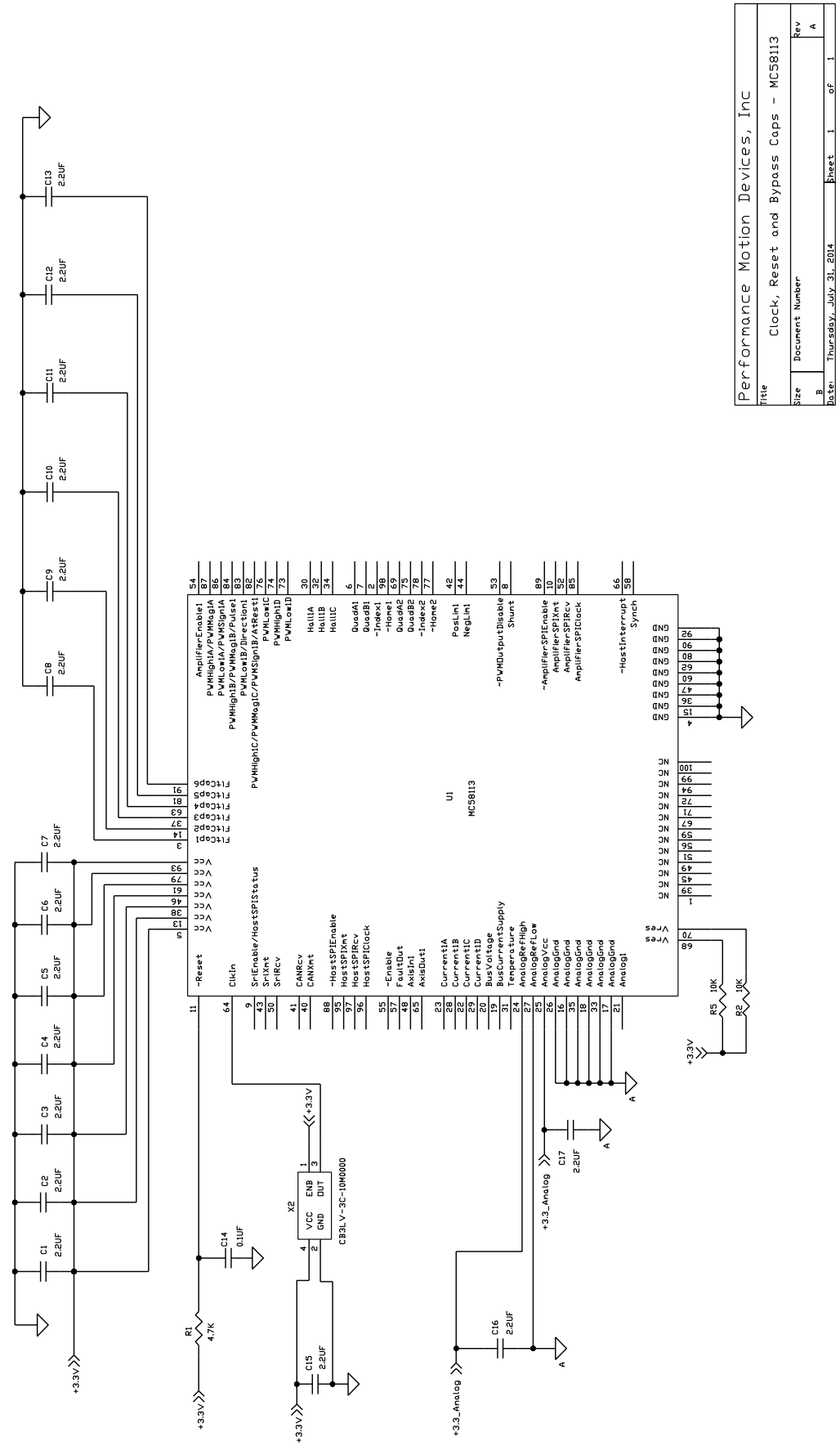
The same points should be considered when designing the ground. A good board layout practice should have a star connection at one point in the power supply.

Additional filtering, such as ferrite beads, may be inserted between the analog and digital grounds to suppress high frequency ground noise. Some components, such as motor drivers, require special grounding. The system designer should refer to the component data sheets of selected components in order to ensure correct usage of the grounding methods.

7.4.3 Decoupling of the On-chip ADC

The voltage supply to the ADC should be decoupled with a 2.2-µF ceramic capacitor (typical) on the pin. It should be placed as close as possible to the ADC power supply input pins. For additional isolation purposes an additional ceramic capacitor can be placed across *AnalogRefLow* and *AnalogRefHigh*.

Figure 7-2: Basics, Clock and Bypass Caps, 58113



7.5 Reset Signal

The MC58113 chip has a built-in power supervisory circuitry that generates an internal reset signal when a power-on or brown-out condition occurs. As such, no external circuitry is needed to generate a reset input pulse. An R-C circuit must be connected to this pin for noise immunity reasons.

The supervisor reset release delay time is typically 600 μsec after the power-on or brown-out condition event is removed. If need be, an external circuit may also drive this pin to assert a device reset. In this case, it is recommended that this pin be driven by an open-drain device.

All digital output signals have an internal pullup except for the following signals: : *AmplifierEnable I , FaultOut,* and *SrlEnable.* The signals are pulled up after a reset but not during. If the *AmplifierEnable I* and *FaultOut* signals are used they should have an external pull down resistor to prevent any glitches during reset.

During the initialization period, the MC58113 is configured with the default initialization parameters for motor type, serial communication and CAN communication, analog offsets, control loop gains etc. If necessary, the MC58113's on chip non-volatile storage can be used to store user-programmed initialization parameters. Please contact PMD to learn more about this option.

7.6 Serial Communication Interface (SCI)

In this section the serial communication interface to the host is described. On power-up or after a reset, unless the on board non volatile storage has been used to store alternate defaults, the MC58113 configures the SCI to its default configuration of 57,600 baud, no parity, one stop bit, point-to-point mode.

This section demonstrates the use of RS-232 and RS-485 line-drivers for interfacing to a remote host.

7.6.1 Asynchronous Serial Communications

When the host and motion control IC are located on the same physical board it is most likely that simply wiring the transmit and receive lines directly between the host and MC58113 chip is all that is required (assuming they are both 3.3V CMOS devices).

For communications between cards or modules TIA/EIA standards provide reliable communication over varying cable lengths and communication rates. The most commonly used standards are RS-232 and RS-485. These standards are separated into two categories: single-ended and differential. RS-232 is a single-ended standard allowing for moderate communication rates over relatively short cables. RS-485 is differential, offering higher data rates and longer cable runs.

Line drivers and receivers (transceivers) are commonly used in order to mediate between the cable interface and the digital circuitry signal levels. There are several design considerations that should be taken into account when deciding which of these two communication methods is the best fit for an application.

- Full-duplex vs. half-duplex

  The terms full-duplex and half-duplex are used to distinguish between a system having two separate physical communications lines from one having one common line for transmission and reception.

- Line contention

  This problem can occur in half-duplex systems. Most line-drivers supply physical protection against such conditions but there is no automatic recovery of lost data in these levels. When interfacing the MC58113

to a half-duplex communication system the designer should note that the turn-around time for command processing and response is at least 1 byte at the current baud rate. As a result the host should release the communication line before this time elapses so that contention can be avoided.

- Termination impedance

  Long cables and/or high data rates require termination resistors if the transceiver is located at the end of the transmission lines. One way to determine if termination is required is if the propagation delay across the cable is larger than ten times the signaling transition time. If this condition is satisfied, then termination is required. The RS-485 standard specifies the signaling transition time to be less than 0.3 times the signaling period, thus imposing an upper limit on the maximum cable length for a specified baud rate.

  The termination resistor should match the characteristic impedance of the cable with 20% tolerance. Resistors with a value of 80-120 are typically used. Note that for transceivers placed in the middle of the cable, no termination resistors are required. However, the stubs should be kept as short as possible to prevent reflections.

The schematic in Figure 7-3 employs the ADM3202 and ADM3491 transceivers as an example of RS-232 and RS-485 interfaces respectively. Other RS-232 transceivers may be used, such as Maxim's MAX3321E. The ADM3491 circuitry can be configured for both full-duplex and half-duplex communications, and may include termination resistors. As an alternative, transceivers from the MAX307xE family may be used.

The following table shows configuration options for the RS-485 circuitry of Figure 7-3:

Configuration	Jumper Position	Application
Half Duplex[1]	JP1/2/3 in 2-3	RS-485 in multipoint system
Full Duplex	JP1/2/3 in 1-2	RS-485 in point to point system
Termination on[2]	JP4/5 in 1-2	RS-485. For high transmission rates and/or long cable. Only when placed at the end of the cable.
Termination off	JP4/5 in 2-3	RS-485. For low transmission rates and short cable. Or when placed at the middle of the cable.

1. JP3 should only be placed be in the half duplex state (2-3) if multi-point communication is being used.

2. Note that the reference circuitry does not support resistance termination on the transmitting side when operated in full duplex because it is assumed that RS-485 will only be used in the half-duplex configuration.

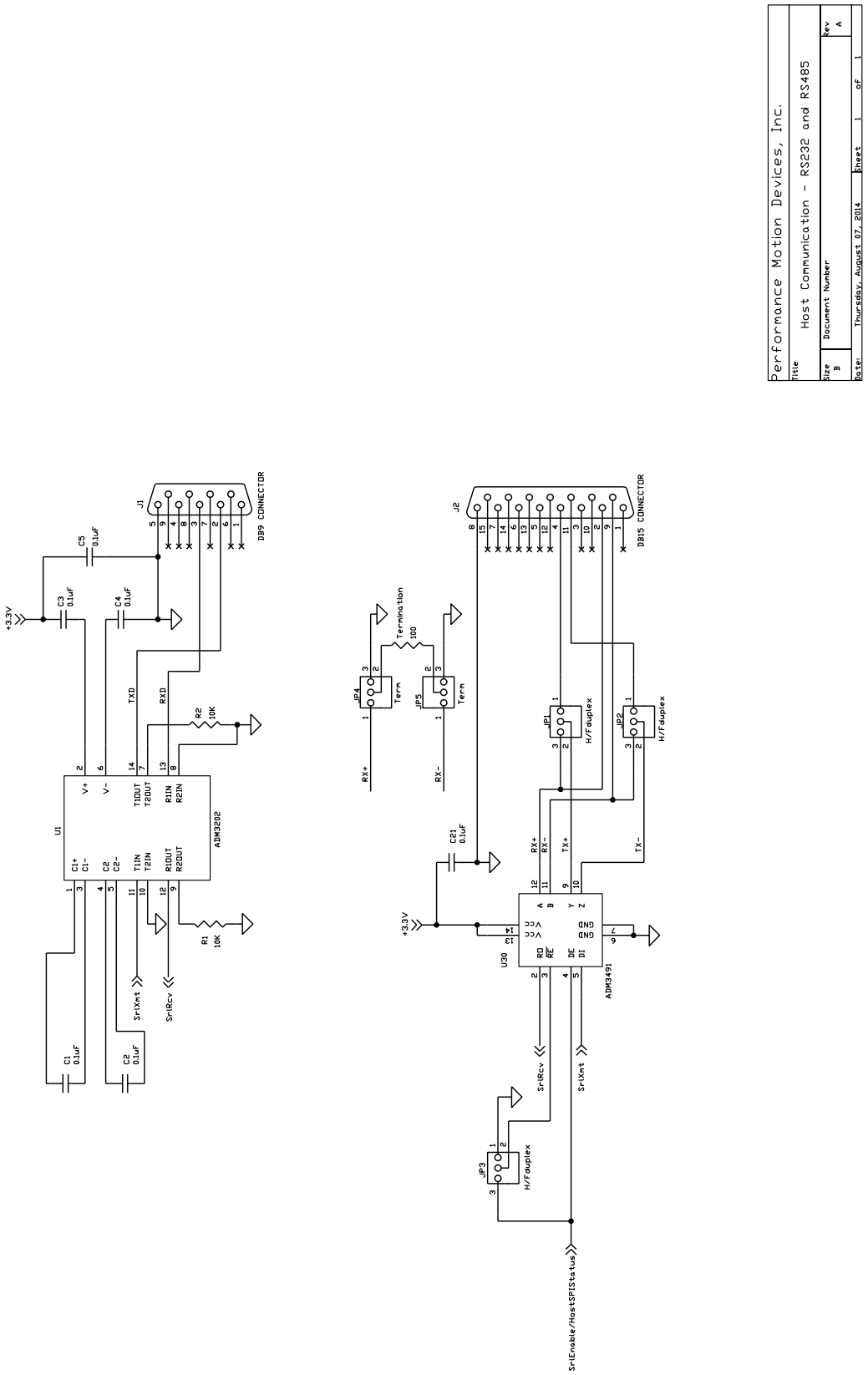


Figure 7-3: Host Communication, RS-232 and RS-485

7.7 CAN Communication Interface

The following example illustrates an interface to a CAN backbone using TI's SN65HVD233 transceiver, which supports the ISO 11898 standard. This port can be operated at various communication rates from 10,000 to 1,000,000 bps (bits per second). In addition, each CANbus device is assigned two CAN identifiers (also called addresses); one for transmission of messages, and one for reception of messages. Generally, the CAN high-speed standard ISO 11898 provides a single line bus structure as a network topology. The bus line is terminated at both ends with a termination resistor of ~120 ohms. However, in practice some deviation from that topology may be needed to accommodate appropriate drop cable lengths for particular applications. Consult CAN ISO 11898 standard for more information on termination schemes and EMC considerations.

7.7.1 CAN Configuration During Power-up or Reset

On power-up or after reset, the MC58113 configures the CAN controller to its default configuration: 20 kbps with a Node ID of 0. The MC58113's on board non-volatile storage can be used to store user-programmed initialization parameters. If a non-default CAN configuration is required, please contact PMD sales representative to learn more. PMD may ship MC58113s pre-loaded with user-specified parameters.

The RS pin of the SN65HVD233 provides for three modes of operation: high-speed, slope control, or low-power standby mode. This programmable input pin may be used to adjust the rise and fall times of the transmitter. This may be important in unshielded, low-cost systems in order to reduce electromagnetic interference. This pin provides three different modes of operation: high-speed, slope control, and low-power modes. The high-speed mode of operation is selected by connecting this pin to ground, allowing the transmitter output transistors to switch on and off as fast as possible with no limitation on the rise and fall slopes. The rise and fall slopes can be adjusted by connecting a resistor to ground at this pin, since the slope is proportional to the pin's output current. This slope control is implemented with external resistor values of 10kohms, to achieve a 15-V/µs slew rate, to 100 kohms, to achieve a 2-V/µs slew rate.

If transmitter's rise/fall times do not require adjusting, the RS pin should be tied to GND or the simpler SN65HVD232 can be used.

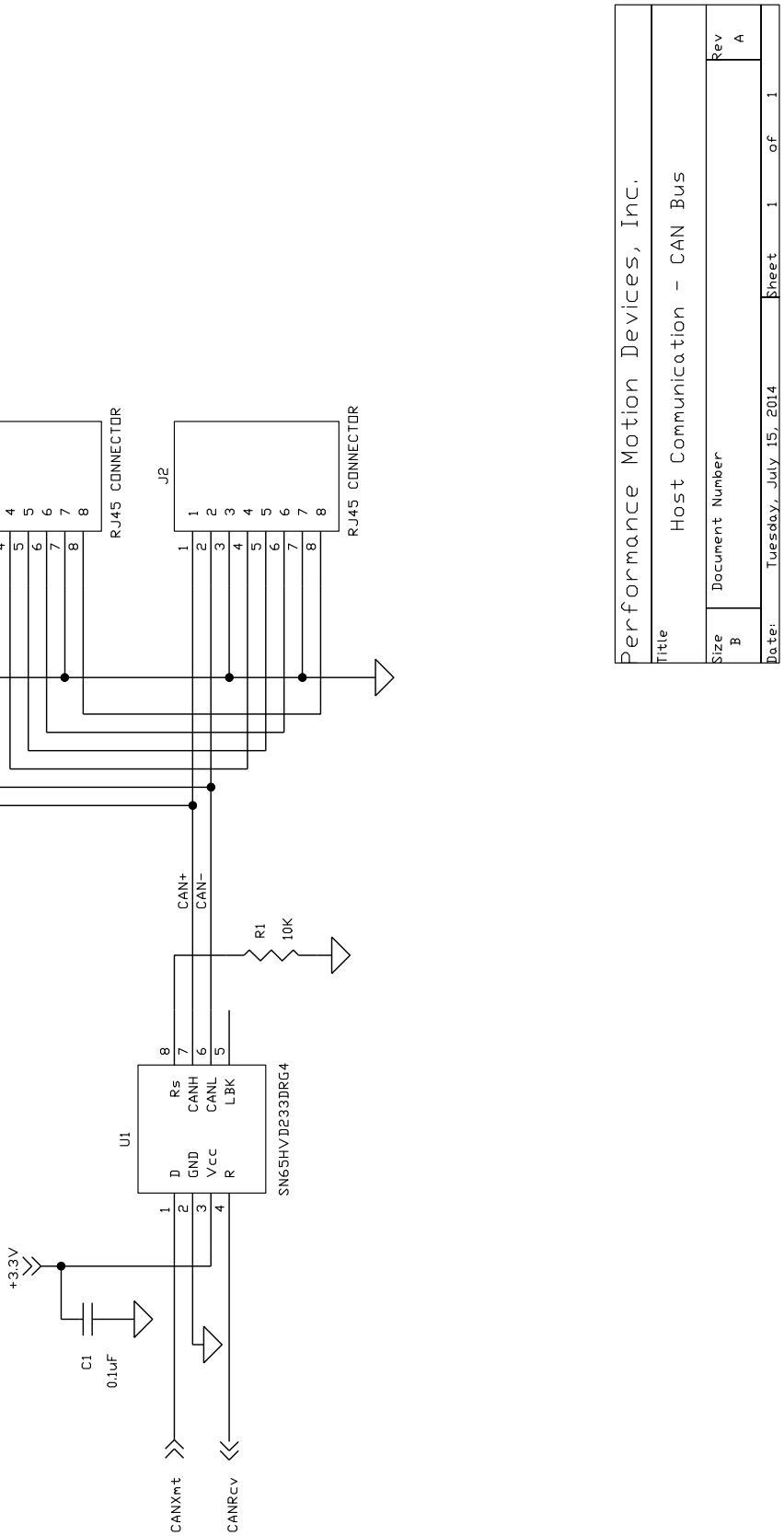


Figure 7-4: Host Communication CANbus

7.8 Host SPI Communication Interface

The MC58113 motion control IC supports SPI (Serial Peripheral Interface) for communications with a host processor such as a microprocessor. The SPI interface is an alternative to the Serial or CAN bus interfaces, and provides fast communication on a single board or over short distances.

The HostSPIClock pin receives the host clock signal. *HostSPIXmt* signal transmits the synchronous serial data to the host, the *HostSPIRcv* signal receives the synchronous serial data from the host processor and the active low *~HostSPIEnable* should be asserted by the host when Host SPI communication is occurring. The normally high *HostSPIStatus* signal is asserted low when the MC58113 is ready to transmit a response. It will return high after the host has read the entire response.

Additional suggestions:

- The host should query the *HostSPIStatus* signal and wait for the proper state before sending a command or reading a response. (Only send a command when *HostSPIStatus* is high, only read a response when *HostSPIStatus* is low).
- When the *HostSPIStatus* signal is low, it will not go high until after the host has read the entire response and de-asserted the ~*HostSPIEnable* signal. The *HostSPIStatus* signal should go high within 25 µs of the de-assertion of the ~*HostSPIEnable* signal.
- If any communication errors are detected the previous command should be repeated. If the *HostSPIStatus* signal is low, the host will need to do a 16-bit transaction before resending the command.
- After the **SetOperatingMode** command has been sent, the host should wait at least 150 µs before sending the next command.
- The effects of **SetSignalSense** command may take 100 µs to appear.
- In most cases, the *HostSPIStatus* signal will go low within 50 µs of the command from the host being received. However some commands (ex. **SetMotorType**) could take up to 200 µs.

The following example schematic in Figure 7-5 illustrates the Host communication via the SPI ports. The host controller is the Microchip's dsPIC33FJ64GS606. The microcontroller's SPI port is used for the host SPI communication.

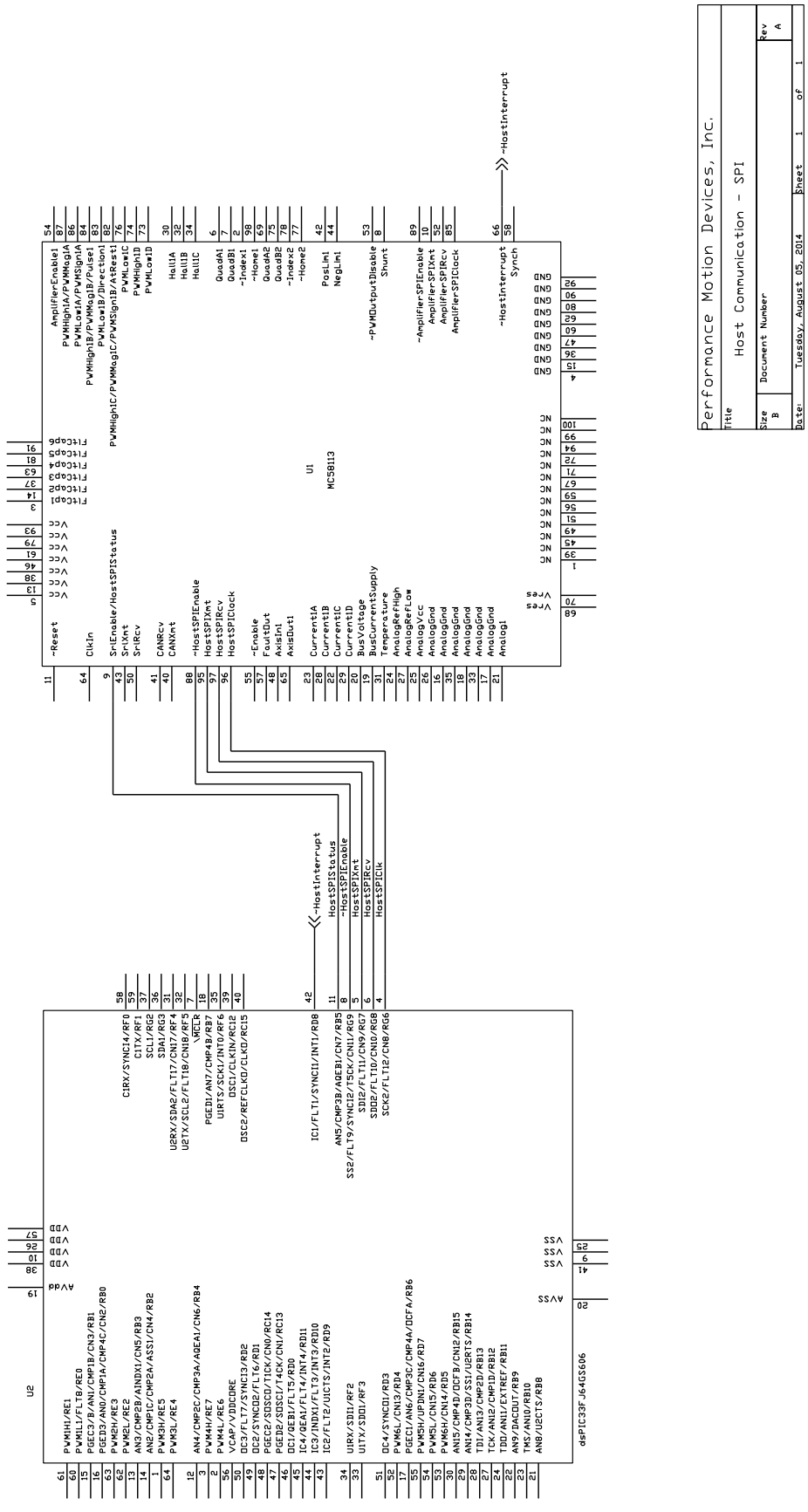


Figure 7-5: Host Communication SPI

7.9 General Purpose Analog Input

In this section two types of conditioning circuits which interface to the MC58113's Analog1 signal are demonstrated. The first circuit interfaces to a single-ended voltage signal, and the second circuit to a differential voltage signal. The conditioning circuits should be adjusted appropriately in order to meet the system's requirements.

Analog1 is a general purpose ADC input. The signal input range needs to fall between ***AnalogRefHigh*** and ***AnalogRefLow*** for normal ADC conversion. Meanwhile, the recommended input range is between ***AnalogVcc*** and ***AnalogGND*** for proper device operation. If the input signal is out of the range, a clamping diode might be necessary for protection.

7.9.1 Using the On-chip ADC

The MC58113 is equipped with a 12-bit ADC. The ADC converts from 0 to AnalogVcc fixed full scale range and supports ratio-metric V_{REFHI}/V_{REFLO} references.

The digital value derived from the input analog voltage is determined using the following formula.

Digital value = 0 when input is <= 0V

Digital value = 32,768 x (input voltage - V_{REFLO}) / (V_{REFHI} - V_{REFLO}) when 0V < input < V_{REFHI}

Digital value = 32,767 when input >= V_{REFHI}

Where V_{REFLO} and V_{REFHI} are the voltages applied at ***AnalogRefLow*** and ***AnalogRefHigh*** pins, respectively. ***AnalogRefHigh must not exceed AnalogVcc.***

The ADC power supply should be decoupled with a low-ESR capacitor. For example, place a 2.2 μF ceramic capacitor or a 2.2-6.8 μF tantalum capacitor in parallel with a 0.01-0.1 μF ceramic capacitor as closely as possible to the power supply and ground pins. An additional low-ESR capacitor may be placed across ***AnalogRefLow*** and ***AnalogRefHigh***.

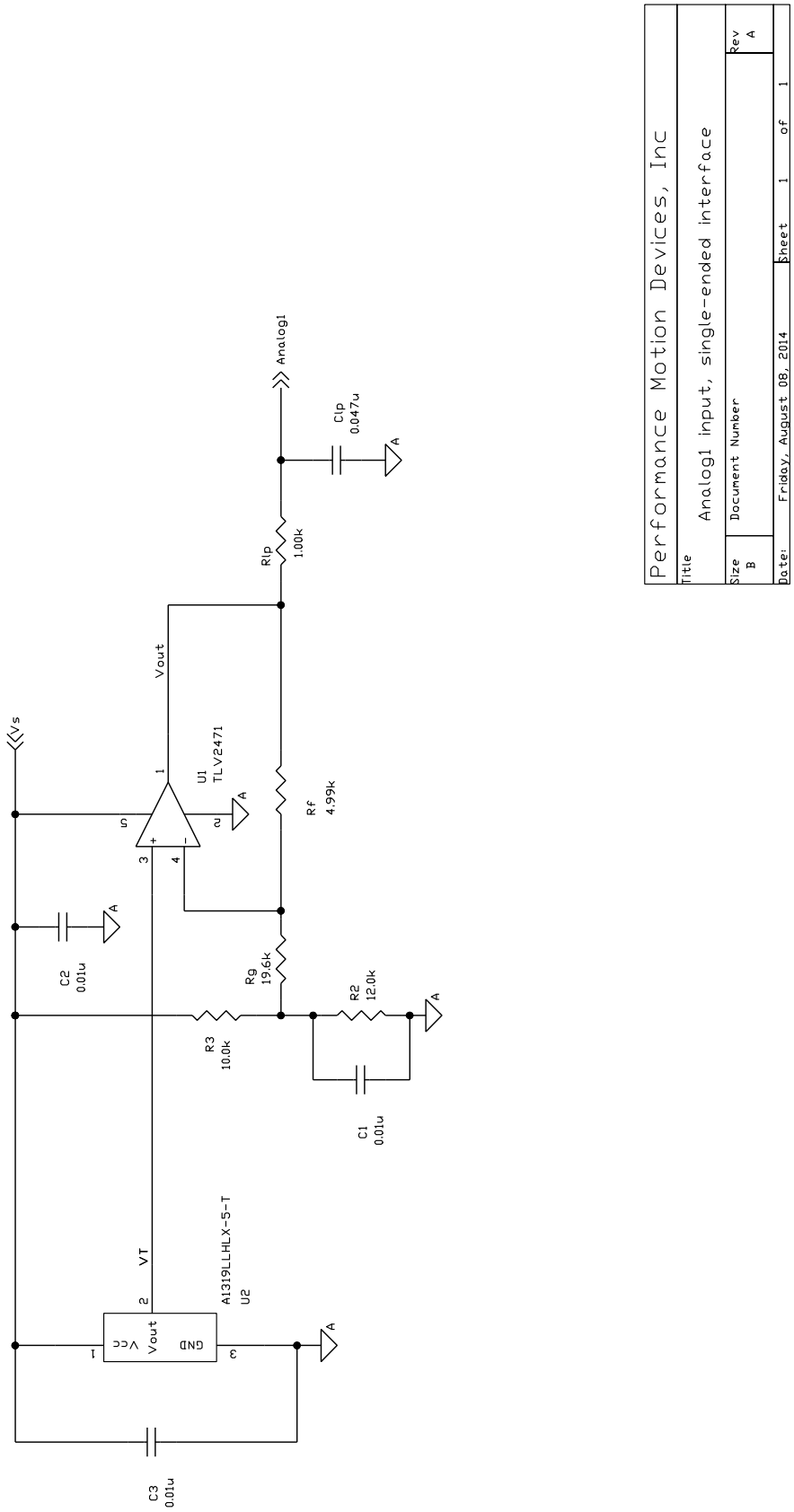


Figure 7-6: Analog Input Single-ended Interface

7.9.2 Single-ended Interface

Figure 7-6 shows a single-ended conditioning circuit that may be used for interfacing a linear Hall-effect sensor, Allegro MicroSystems A1319. The input signal, V_T, is a single-ended voltage signal. It is assumed that its output range be 0.45 - 2.9V and vary slowly, at no greater than 100 Hz.

The goal of the conditioning circuitry is to match the analog signal to the ADC's voltage range and supply it with the required power. The conditioning circuit should be kept as simple as possible and make use of a single +3.3V supply.

7.9.2.1 Conditioning Circuitry and Op-amp Selection

Because the input is a voltage signal, an inverting amplifier is used to ensure a large input impedance. The operational amplifier should have rail-to-rail inputs/outputs with a unipolar supply. The TLV2471 is used here as it can swing to within 180 mV of each supply rail while driving a 10 mA load.

The functionality of the circuitry at DC is depicted in equation (1).

$$Vout = V_T\left(1+\frac{Rf}{Rg+R_3\|R_2}\right)-Vs\cdot\frac{R_2}{R_2+R_3}\cdot\frac{Rf}{Rg+R_3\|R_2} \qquad (1)$$

Where Vs is the AnalogVcc, and in this example, it is set at 3.3V.

The gain of the circuitry is calculated in this manner so as to accommodate the full output swing of the op-amp, and to match it to the input swing of V_T. This is shown in the following equation.

$$\left(1+\frac{Rf}{Rg+R_3\|R_2}\right)=\frac{3.3-2\cdot 0.18}{2.9-0.45}=1.2 \qquad (2)$$

Additionally, the circuitry should bias the output so that when V_T reaches the lowest value of interest, the op-amp also reaches its lowest output voltage. Applying (2) and calculating equation (1) at Vout = 0.18, and V_T = 0.45 results in the following.

$$\frac{R_2}{R_2+R_3}=0.5455 \qquad (3)$$

Selecting R_2 = 12k (1%), R_3 = 10.0k (1%), Rg = 19.6k (1%), Rf = 4.99k (1%) satisfies equations (2) and (3), while maintaining load currents in the working range of the op-amp and ADC.

Note that if the input voltage V_T is ratiometric with respect to the supply voltage Vs, then the variation and sensitivity of the circuitry in Vs is relatively small since the same variations will affect the ADC. This will cancel out the variation's effects on the conditioning circuitry.

7.9.2.2 Rlp and Clp values

A low-pass RC filter is used to eliminate noise and prevent aliasing. Additionally, it is used to limit the load on the op-amp, which enables it to swing as close as possible to its rails.

Using Rlp = 1 kohms and a ceramic Clp = 0.047 µF will result in a low-pass filter with a 3 dB point at f_0~3 kHz (which is assumed to be at least one order larger than the signal's bandwidth). The capacitor should be placed as close as possible to the ADC input pin, as it partially drives the sample capacitor of the ADC.

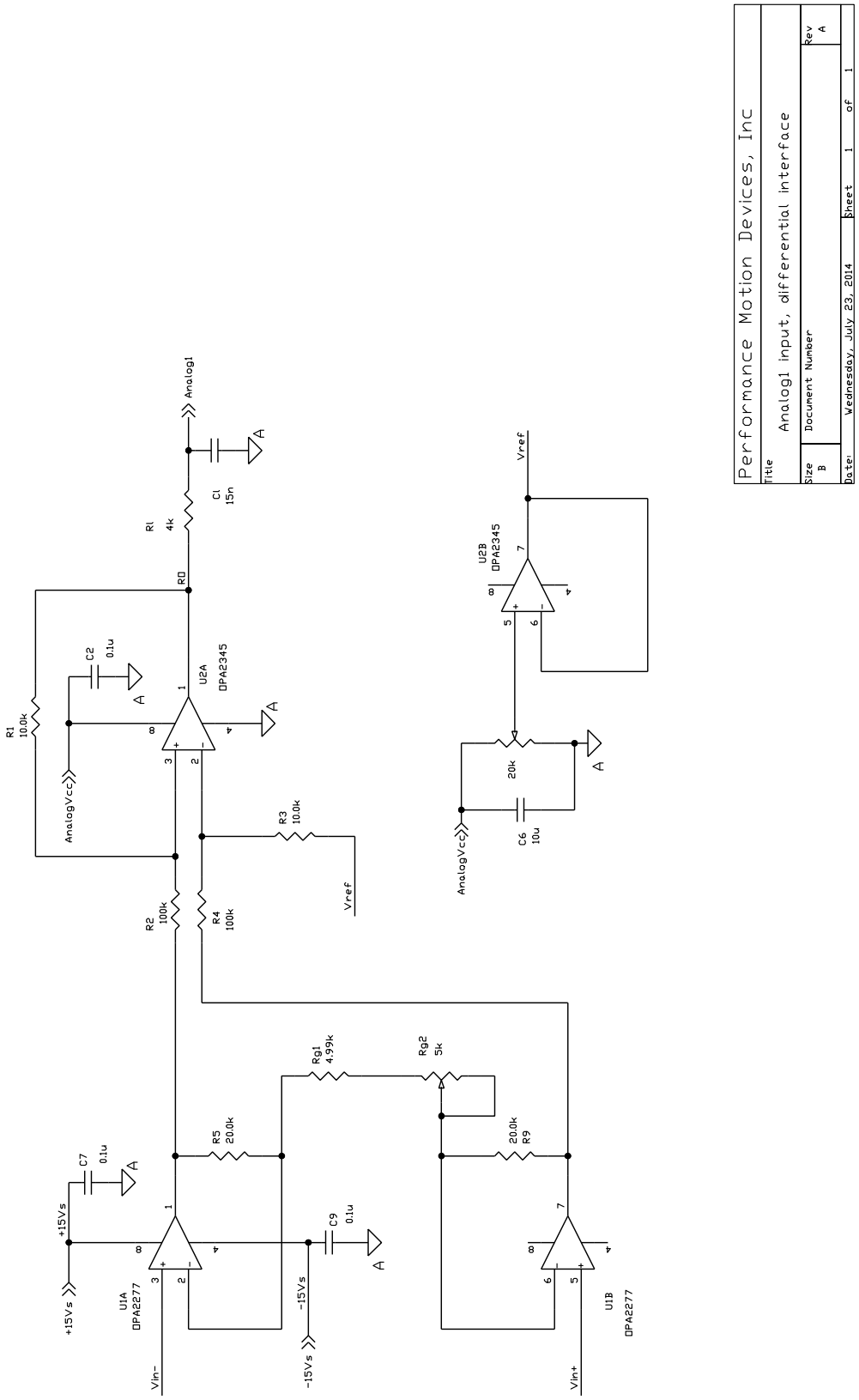


Figure 7-7: Analog Input Differential Interface

7.9.3 Differential Interface

Figure 7-7 shows a differential signal conditioning circuit. The input signal is assumed to be differential, Vin+ and Vin-. The voltage signal is in the range of (Vin+ - Vin-) = (-3V, +3V), and slowly varying (not greater than 100 Hz).

The goal is to condition the differential input signal to fit the ADC's voltage range, and supply it with the required drive. For example, the circuitry may be used to interface to a Resonator Rate Sensor such as the RRS75 from Inertial Science, Inc. Additional ADC channels may be used simultaneously in order to expand the dynamic range of the ADC.

7.9.3.1 Conditioning Circuitry

The purpose of this interface is to generate a signal with the following format.

Analog1 = G(Vin+ - Vin-) +Vref, with nominal G = 0.55 and Vref = 1.65.

The interface shown in Figure 7-7 forms an instrumentation amplifier. The high input impedance of the instrumentation amplifier is highly desirable to eliminate voltage drops and CMRR concerns due to the signal source output impedance.

The following equation describes the functionality of the conditional circuitry at DC.

$$RO = (Vin+) \cdot G - (Vin-) \cdot m + Vref \cdot [(R_2+R_1) / R_2] \cdot [R_4 / (R_3+R_4)] \quad (5)$$

where:

$$G = [R_1 / R_2] \cdot [(R_5+R_g) / R_g] + [R_6 / R_g] \cdot [R_3 / (R_3+R_4)] \cdot [(R_2+R_1) / R_2]$$

$$m = [(R_6+R_g) / R_g] \cdot [R_3 / (R_3+R_4)] \cdot [(R_2+R_1) / R_2] + [R_1 / R_2] \cdot [R_5 / R_g]$$

Selecting $R_3 = R_1$ and $R_4 = R_2$ will result in the following simplified version:

$$RO = (Vin+ - Vin-) \cdot [R_1 / R_2] \cdot [1+ (R_5+R_6) / R_g] + Vref \quad (5a)$$

Specifying resistors $R_3 = R_1$ = 10.0 kohms (%1), $R_4 = R_2$ = 100.0 kohms (1%), $R_5 = R_6$ = 20.0 kohms (1%), and nominal R_g = 8.9 kohms, will result in the desired G = 0.55. The importance of having matching pairs of resistors should be evident from equation (5). If matching is not done common mode voltage will be introduced.

The OPA234 (5) is an input/output rail-to-rail operational amplifier with low voltage bias, and high CMRR. It tolerates input common voltages of ± 0.3V from its rails. As a protection measure, the addition of Shottky diodes with 0.3V forward voltage, such as 20L15T, is recommended (but not shown). The output swing of the op-amp is closely related to the load current. In order to make this current as low as possible, a resistor is added at the output of the op-amp. Adding a capacitor forms a LPF, with a 3 dB cut-off at ~3 kHz. The capacitor should be placed as close as possible to the ADC input pins, and is partially used to drive the sampling capacitor.

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7.10 Drive-Related Safety and Monitoring Features

This example shows the motor drive-related analog monitoring features. Please refer to Section 7.12, "PWM High/ Low Motor Drive With Leg Current Sensing/Control," for leg current sensing functions.

The block of R9, R10, R13 and C5 is for temperature sensing. R13 is a thermistor, and its resistance depends on the temperature. MC58113 will sense the scaled voltage and convert it into temperature reading. C5 need to be tied close to the Temperature pin to improve noise immunity.

In this example, it is assumed that the thermistor is away from the MC58113 and close to the power train, which usually has the highest temperature. Accordingly, C5 is referred to the analog ground, and R13 to digital ground. R10 is optional to improve the noise immunity. If R13 is close to the analog portion, Vcc can be AnalogVcc instead and R13 be tied to the analog ground.

The block of R2, R3, R5 and C3 is for input voltage sensing. This voltage divider will scale the +HV into the range between ground and ***AnalogRefHigh***. In this example, it will scale 63V to 3.3V. C3 need to be tied close to BusVoltage pin. The voltage divider is referenced to digital ground while C3 is to analog ground. An optional resistor can be put between R5 and C3 to improve noise immunity as R10 does for temperature sensing function. This block is also a low-pass filter with bandwidth of 1.8kHz. This bandwidth should be selected to respond to real voltage fault event while attenuating bus noise.

U1 is the high side bus current sensing IC. With current sensing resistor R1 at 10mOhm, U1 has a current scaling factor of (13.3/2*0.01)=66.5mV/A.

U2A is for short circuit protection. R12 and R7 set the protection trigger point, and R6 provides a hysteresis. When Vcc is 3.3V, the trigger point is 1.65V with hysteresis. ***~PWMOutputDisable*** will go to low and trigger protection when U1 output is over 1.65V, which is (1.65/66.5mv/A)= 25A.

The output of U1 also goes to U3A, which is a peak-detection circuit. MC58113 will sample the analog input at 20kHz. The peak-detection circuit will hold the maximum peak current reading between the sampling points so MC58113 can detect the maximum current. The necessity of this peak-detection circuit depends on the power train design. For example, if C1 and C2 have big enough capacitance so that the current in R1 will be close to DC, U3A can be a buffer instead.

MC58113 support leg current sensing with current loop control, and R11 and R15 are leg current sensing resistors.

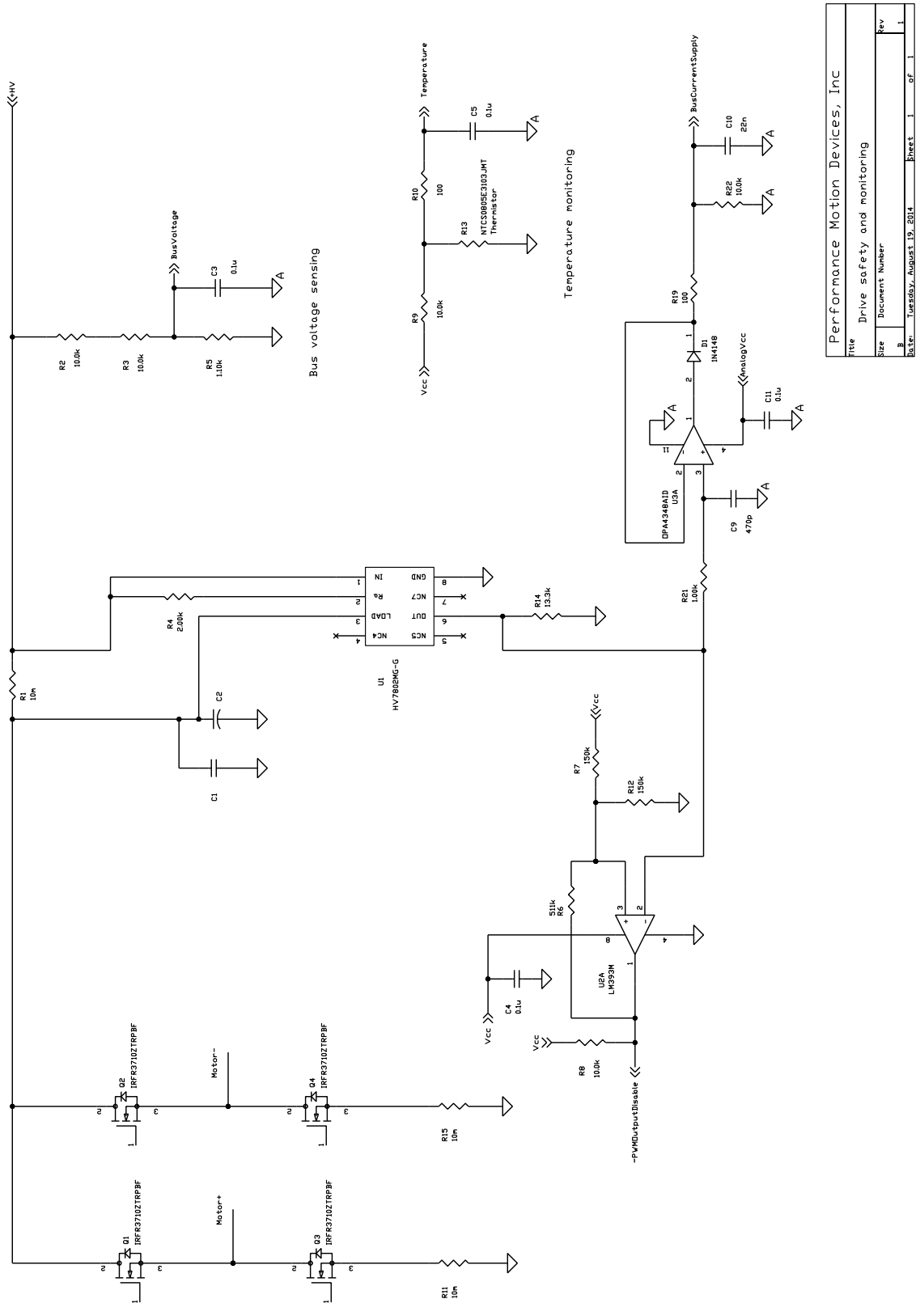


Figure 7-8: Drive Safety and Monitoring

7.11 Shunt Resistor Drive

This example shows shunt function driving a dynamic brake resistor.

The power train driven by the MC58113 is capable of regeneration. It could harvest the mechanical energy during slow down or direction reversion and transfer the energy back to the power input. When the input power supply cannot handle the regenerative power, input voltage +HV will go up and over-voltage is possible. The Shunt pin can implement dynamic braking, which will converts the energy into heat and controls the +HV voltage.

The shunt signal is controlled based on the input voltage sensing, and it will become active when input voltage is too high.

Shunt is a PWM-based signal and drives MOSFET Q1 through driver U1. When Q1 is turned on, current will flow through R1 and consume energy. When Q1 is turned off, D1 will provide a free-wheeling path for the current in R1 decaying to zero. Q1 and D1 should be sized to handle the current. Also, R1, Q1 and D1 should be sized to handle both the instantaneous power and average power during braking operation.

Upon power up or during reset, Shunt pin is high impedance. In this example, U1 has internal pull-down resistor to ensure Q1 being off. If different driver is used, a pull-down or pull-up resistor might be necessary to ensure the shunt function be off for safe power up and reset.

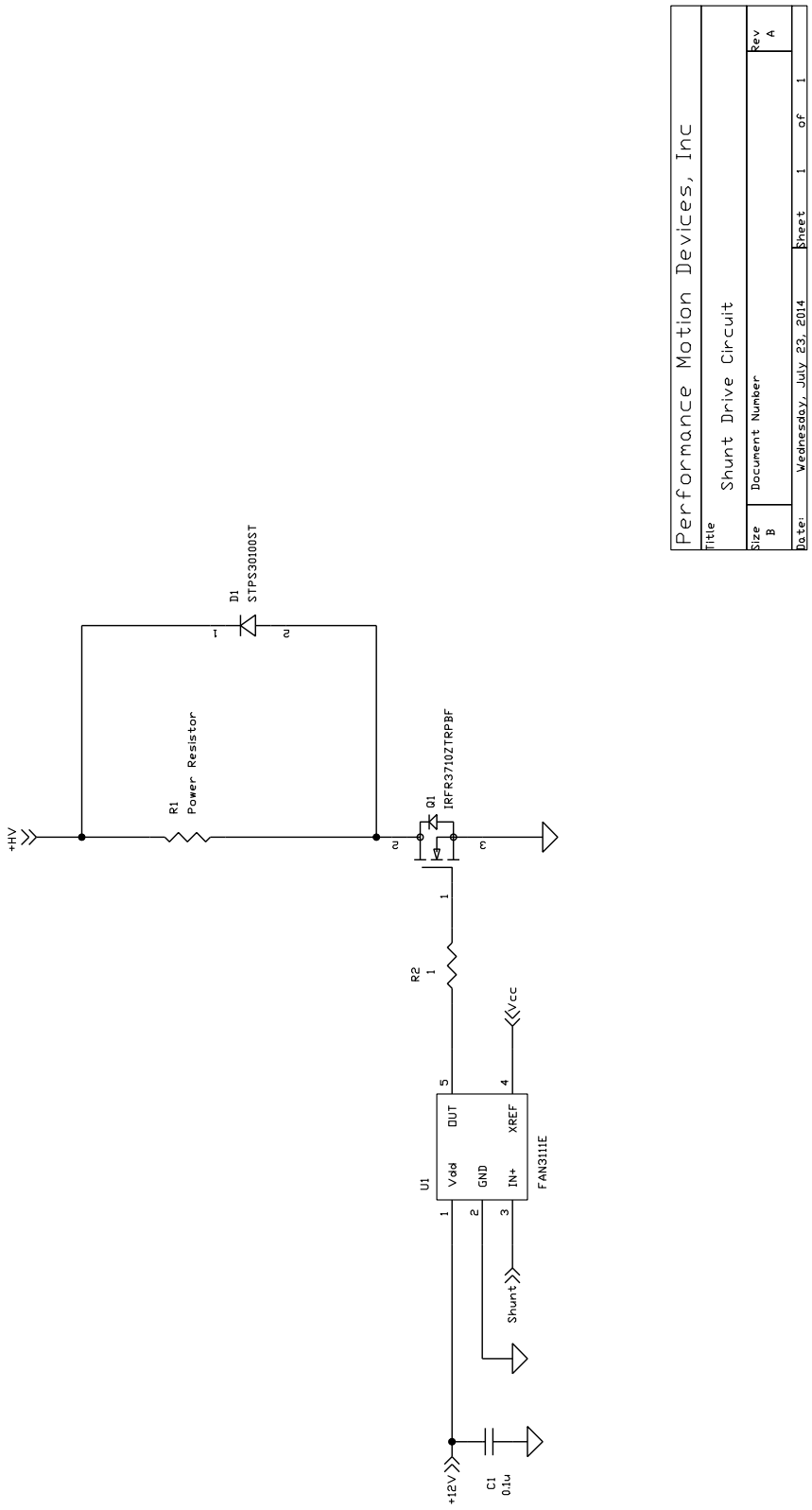


Figure 7-9: Shunt Drive Circuit

7.12 PWM High/Low Motor Drive With Leg Current Sensing/Control

This section presents several design examples PWM high/low motor drive with leg current sensing. The examples focus on different priorities including power rating, cost, and noise immunity. Also, although specific motor type is shown in the examples, the design considerations apply to all motor types.

7.12.1 Leg Current Sensing

Figure 7-10 shows an example for leg current sensing. Only phase A is shown here while the design for other legs are the same.

This example has two functional sections. The first is the current sensing sensor, and the second is the analog signal conditioning circuit.

In this example, the leg current sensor is a resistor, R2. Q1 and Q2 are the half-bridge power train for motor winding phaseA. Current sensing resistor R2 senses the leg current in Q2, which equals the motor winding current when Q2 conducts.

Q2 is switching at the PWM frequency, and the voltage drop on R2 is proportional to the motor winding current when Q2 is on. Therefore, the voltage signal is also a chopping signal. MC58113 always sample the signal when Q2 is on to ensure an accurate reading. Also, the voltage drop can be positive, negative or zero depending on the winding current direction.

U1 and the passive parts are the analog conditioning circuit. It scales and filters the voltage signal on R2 and input to the MC58113 ADC input pin Current1A.

U1A is configured as a differential amplifier with R3=R5 and R1=R6. It amplifies the voltage drop across R2, which is the differential voltage. It also attenuates the common mode noise including the noise on the power train.

U1B provide a voltage bias source as half the *AnalogRefHigh*. This bias can be shared with current sensing stages of other phases. *AnalogRefHigh* is the reference voltage to MC58113's ADC reference high. With this voltage bias, MC58113 can sense R2 current in either direction. Other ways to generating this bias voltage is to use voltage reference such as TLV431 or resistance matching.

By default, the MC58113 takes (*AnalogRefHigh*/2) reading as zero current. The MC58113 provides commands to compensate the error introduced by the offsets and tolerances of the current sensing circuit.

R4 and C1 is a low pass filter to reduce output noise. It also alleviates the signal glitch due to ADC sampling. R4 and C1 have to be placed close to MC58113 Current1A pin. Please note, because the signal on R2 is a chopping signal at the PWM frequency, the bandwidth of R4 and C1 should be much higher than the PWM frequency preventing signal distortion/delay.

The gain of the current sensing circuit is

$V_{Current1A}$ = I_leg*R2*R1/R3+AnalogRefHigh/2

When AnalogRefHigh is 3.3V, this example has

$V_{Current1A}$ = I_leg*0.02*54.9/10.0+3.3/2= 0.1098*I_leg+1.65

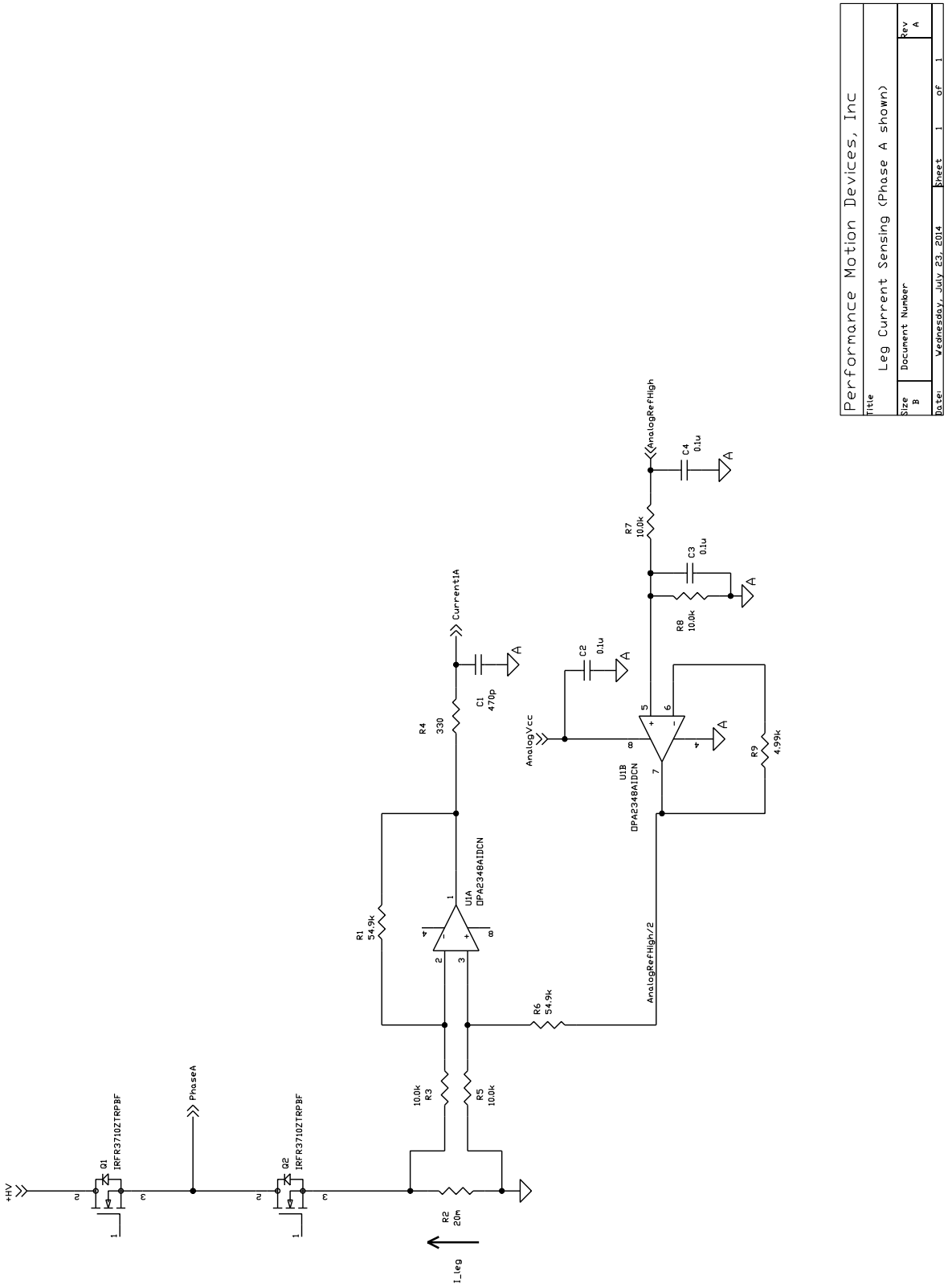
I_leg is defined as positive flowing from the ground to Q2 as shown in the schematic. It is because the current out of the half bridge and into motor winding is defined as positive.

Therefore, when *AnalogRefHigh* is 3.3V, the current sensing range is ±15A. This current range should include the peak current during dynamic regulation. For example, during acceleration, the instantaneous current could be twice of the continuous current or even more.

With the continuous current and peak current known, the power rating of the current resistor can be determined. The conservative design rule is to assume that the current will go through R2 continuously, and the power dissipation is $I^{\wedge 2}*R_2$. However, the current will only flow through the resistor when Q2 is on; that is, if the duty cycle is known for this leg, the power dissipation can be approximated as $I^{\wedge 2}*R_2*(T_{Q2ON}/T_{PWM})$ and resistor can be sized accordingly.

The board layout is critical for an optimal current sensing signal. The current sensing traces (to R3/R5) should be separated from the power path through R2, and these two traces should be routed in pair to improve its common-mode noise immunity. Also, a motor power train has multiple current sensing resistors, and these resistors are referred to ground. During layout, please treat those ground traces (e.g. trace to R5) as separated traces for each leg.

Figure 7-10: Leg Current Sensing



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7.12.2 Low Cost DC Motor Drive

This example presents a low-cost, high performance DC motor drive.

The power train shown is an H-bridge (two half-bridge) for DC motor winding Motor+ and Motor-. The input voltage can be up to 24V. It is capable of driving 1A continuous current with peak current of 2A.

The design for the two half-bridges and their current sensing circuits are the same. Using Motor+ as an example, the half bridge has a P-channel MOSFET as the upper switch and an N-channel MOSFET as the lower switch, which is driven by PWMHigh1A and PWMLow1A through buffer U1.

During normal operation, PWMLow1A is active low. A logic "0" will generate 5V output at U1B, which turn on the lower N-channel MOSFET. R15, R7 and D5 provide an unsymmetrical turn-on and turn-off capability.

PWMHigh1A is active high. A logic "1" will generate 0V output at U1A, which will pull C2 to ground. +HV will charge C2 through D1 and R1 with voltage clamped by D1 (5.1V typical). This clamped voltage will turn on the P-channel MOSFET. When PWMHigh1A is "0", U1A outputs 5V, and C2 will discharge and turn off the P-channel MOSFET. R3, D3 and R5 provide an unsymmetrical turn-on and turn-off capability.

The MC58113 allows the user to configure the active polarity of all PWMs.

Upon power up or during reset, PWMHigh1A and PWMLow1A outputs are high impedance. Therefore, pull-up resistor R13 and pull-down resistor R9 are used to ensure that the upper and lower switches are all off. Also, when a hard fault is triggered, PWMHigh1A and PWMLow1A will go into high impedance, and R13 and R19 will turn off the MOSFET and put the output of the half bridge into high impedance.

R11 is the current sensing resistor, and U2A is the differential amplifier for signal conditioning. Please see Section 7.12.1, "Leg Current Sensing," for more design considerations on leg current sensing.

This design has a low BOM cost and a small board footprint suitable for cost-sensitive or size-sensitive applications. However, its limits are also obvious. For example, the MOSFET driver's driving capability is limited by U1, and current capability is limited by the P-channel MOSFET. Therefore, this design is a good candidate for low voltage and low current applications. For higher voltage and higher current applications, please refer to following examples for half-bridge design.

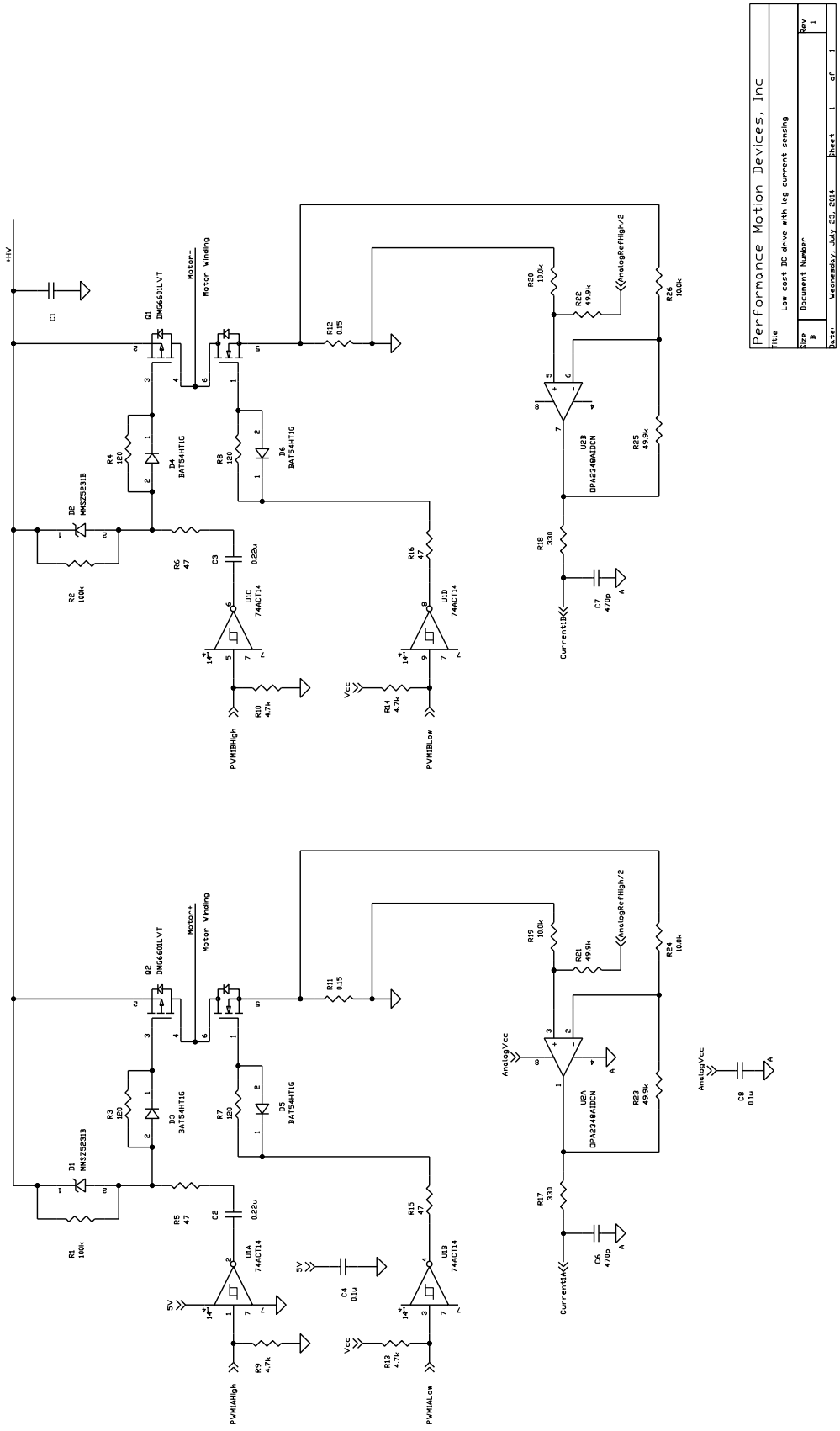


Figure 7-11: Low Cost DC Drive with Leg Current Sensing

7.12.3 Step Motor Drive

This example shows a step motor drive with leg current sensing. The power train has four half-bridges for the step motor's four winding terminals. The input voltage in this example can be up to 56V. It is capable of driving 5A continuous current with peak current of more than 10A.

The design considerations for the four half-bridges and their current sensing circuits are the same. Using PhaseA+ as example, the half bridge uses N-channel MOSFETs for both the higher and the lower switches to achieve high efficiency. The half bridge is driven by PWMHigh1A and PWMLow1A through MOSFET driver U1, which is powered by 12V.

During normal operation, PWMHigh1A and PWMLow1A are active high. For PWMLow1A, a logic "1" turns on the MOSFET Q3. R5, R6 and D3 provide an unsymmetrical turn-on and turn-off capability.

A logic "1" PWMHigh1A will turn on Q1. C3 is the bootstrapping capacitor, and it is charged through D1 when Q3 is turned on. C3 provides the power to turn on Q1, and C3 needs to be a low-ESR capacitor such as a ceramic capacitor. D1 should be a fast switching diode with low leakage current, and its voltage rating should be chosen based on +HV and the +12V. R3 is optional; it can limit the charging current, especially during power up when C3 is zero voltage. R1, R4 and D2 provide an unsymmetrical turn-on and turn-off capability.

Upon power up or during reset, PWMHigh1A and PWMLow1A output are high impedance. Therefore, pull-down resistors R13/R14 ensure that the upper and lower switches are all off so that the half bridge output is high impedance. Also, when a hard fault is triggered, PWMHigh1A and PWMLow1A will go into high impedance, and the pull-down resistors will turn off the MOSFETs and put the output of the half bridge into high impedance. Usually the MOSFET driver has internal pull-up or pull-down resistors, and the user needs to check the driver's datasheet and decide if the resistors are necessary.

R9 is the current sensing resistor, and U3 is the differential amplifier for signal conditioning. Please see Section 7.12.1, "Leg Current Sensing," for more design considerations on leg current sensing.

This design uses dedicated MOSFET drivers and N-channel MOSFETs to achieve high efficiency and high performance. This example provides a balanced design reference between performance and cost for applications up to 56V and current up to 10A. With different MOSFETs, higher voltage and current capabilities can be achieved. Please refer to the low cost DC drive example if cost is critical and to BLDC drive example for high voltage and/or high current applications in noisy environments.

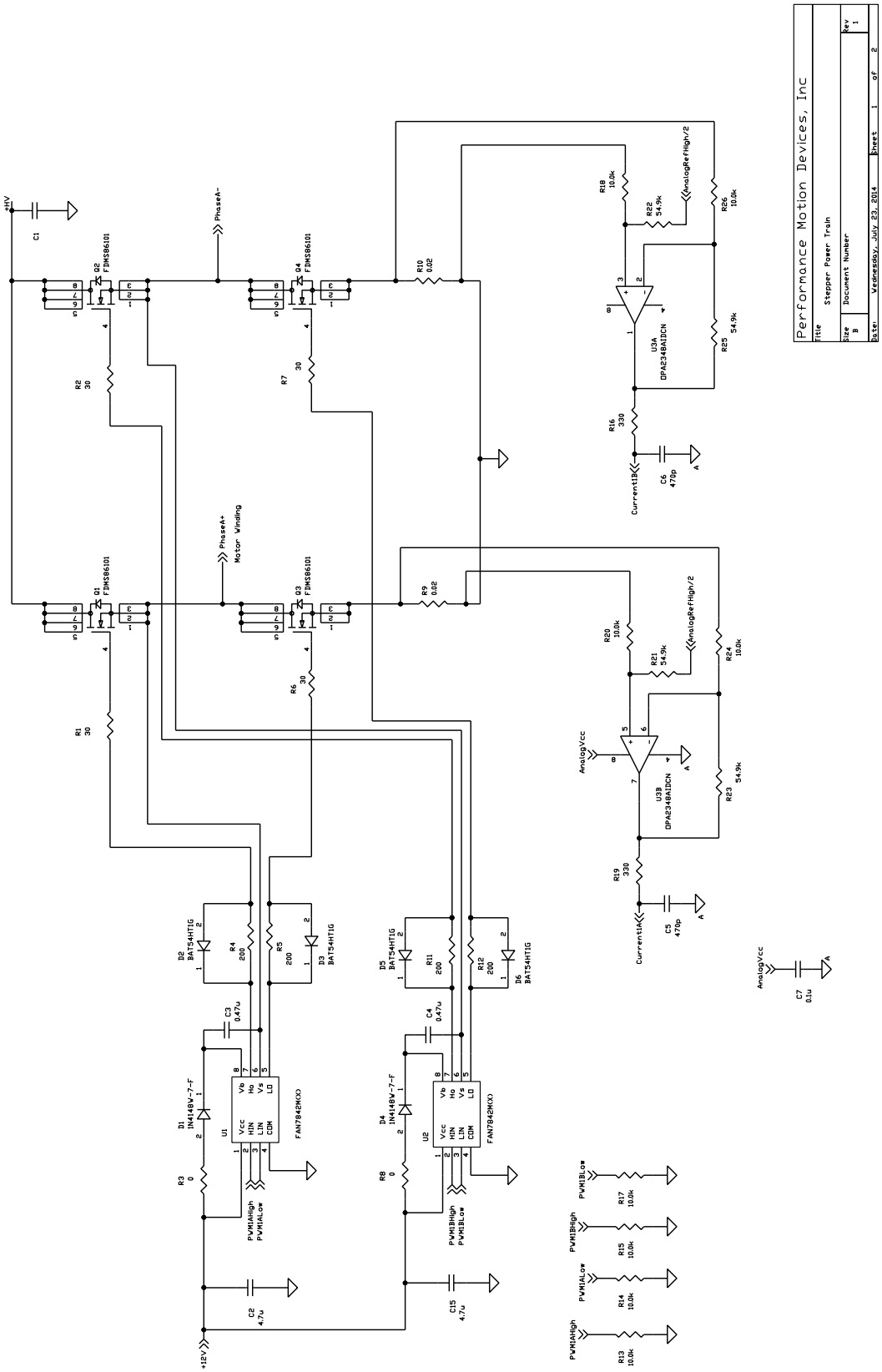


Figure 7-12: Step Motor Drive with Leg Current Sensing

7.12.4 Brushless DC Motor Drive

This example shows a brushless DC motor drive with leg current sensing. The power train has three half-bridge for BLDC motor's three winding terminals. The input voltage in this example can be up to 56V. It is capable of driving 15A continuous current with peak current of more than 25A.

The design considerations for each half-bridge and their current sensing circuits are the same. Using PhaseA+ as example, the half bridge uses N-channel MOSFETs for both the higher and the lower switch to achieve high efficiency. The half bridge is driven by PWMHigh1A and PWMLow1A through MOSFET driver U4, which is powered by 15V.

During normal operation, PWMHigh1A and PWMLow1A are active high. For PWMLow1A, a logic "1" turns on the MOSFET Q3. R25, R26 and D3 provide an unsymmetrical turn-on and turn-off capability.

A logic "1" PWMHigh1A will turn on Q1. C11 is the bootstrapping capacitor, and it is charged through D1 when Q3 is turned on. C11 provides the power to turn on Q1, and C11 needs to be a low-ESR capacitor such as a ceramic capacitor. D1 should be a fast switching diode with low leakage current, and its voltage rate should be chosen based on +HV and the +15V. R23 is optional; it can limit the charging current, especially during power up when C11 is zero voltage. R20, R24 and D2 provide an unsymmetrical turn-on and turn-off capability.

Upon power up or during reset, PWMHigh1A and PWMLow1A output are high impedance. Therefore, pull-down resistors R36 and R37 ensure that the upper and lower switches are all off so that the half bridge output is high impedance.

When a hard fault is triggered, PWMHigh1A and PWMLow1A will go into high impedance, and the pull-down resistors will turn off the MOSFETs and put the output of the half bridge into high impedance. Usually the MOSFET driver has internal pull-up or pull-down resistors, and the user needs to check the driver's datasheet and decide if the resistors are necessary.

The MC58113 has an AmplifierEnable1 output, and it is used to shut down the MOSFET driver through the SD pin. Upon power up or during reset, AmplifierEnable1 is high impedance, and pull-down resistor R19 will ensure all motor output high impedance. When AmplifierEnable1 pin is used, the pull-down resistors R36/R37 are options.

R29 is the current sensing resistor, and U1A is the differential amplifier for signal conditioning. Please see Section 7.12.1, "Leg Current Sensing," for more design considerations on leg current sensing.

This design uses dedicated MOSFET drivers and N-channel MOSFETs to achieve high efficiency and high performance. This example is suitable for applications in high noise environments. The MOSFET driver U4 has two ground references: Vss for the digital side and COM for the power side. The MOSFET turn-on and turn-off current out of pin LO will return from dedicated traces to pin COM instead of ground plane, which makes the board layout easier for noise immunity. The COM connection scheme shown also applies for H-bridge and 3-phase MOSFET driver with dedicated COM pin. For this example with independent half-bridge MOSFET drivers, COM pins can also be connected to respective MOSFET source pins to further improve the driving performance. Please refer to the low cost DC drive example if cost is critical and to the Stepper drive example for general-purpose applications.

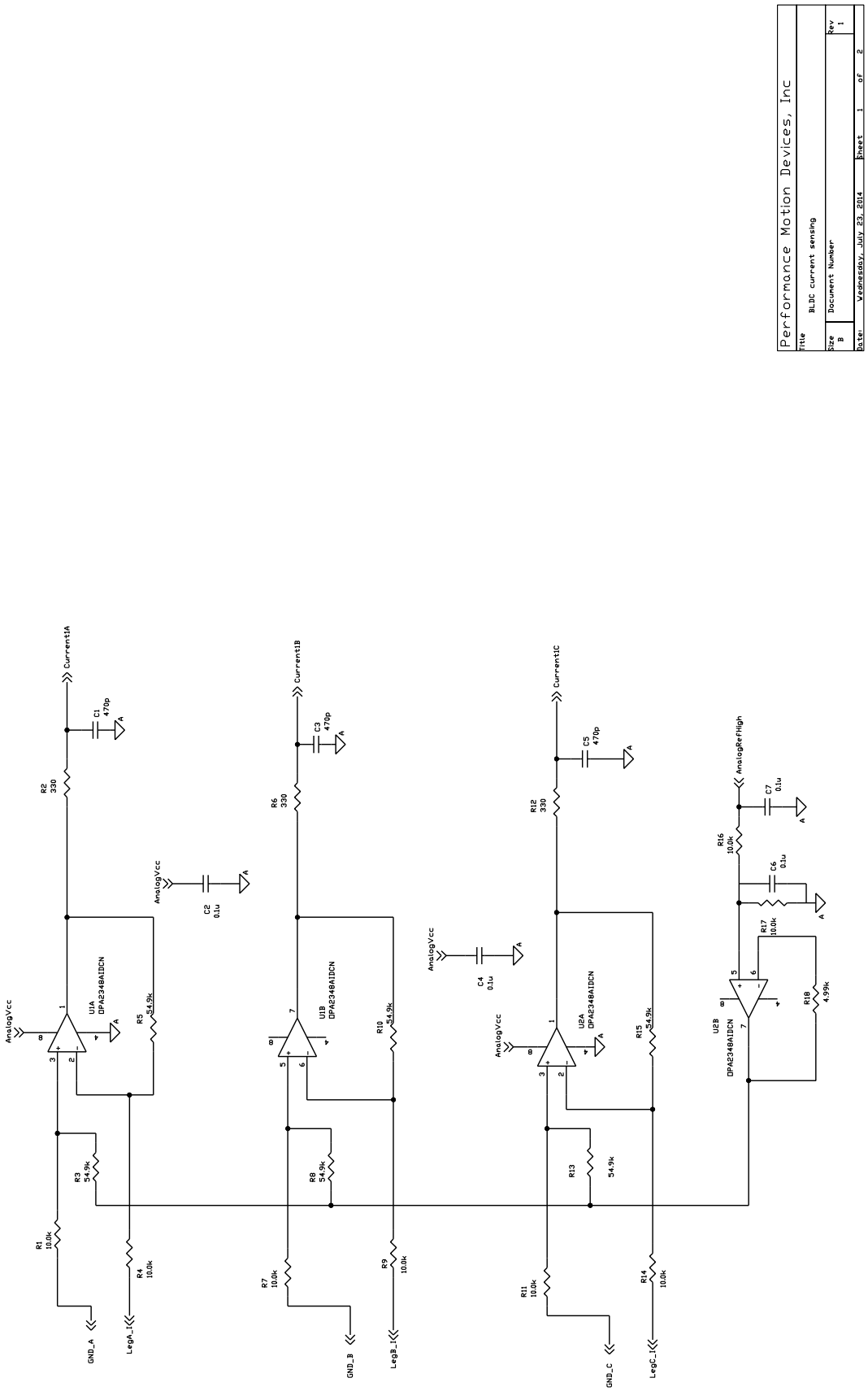
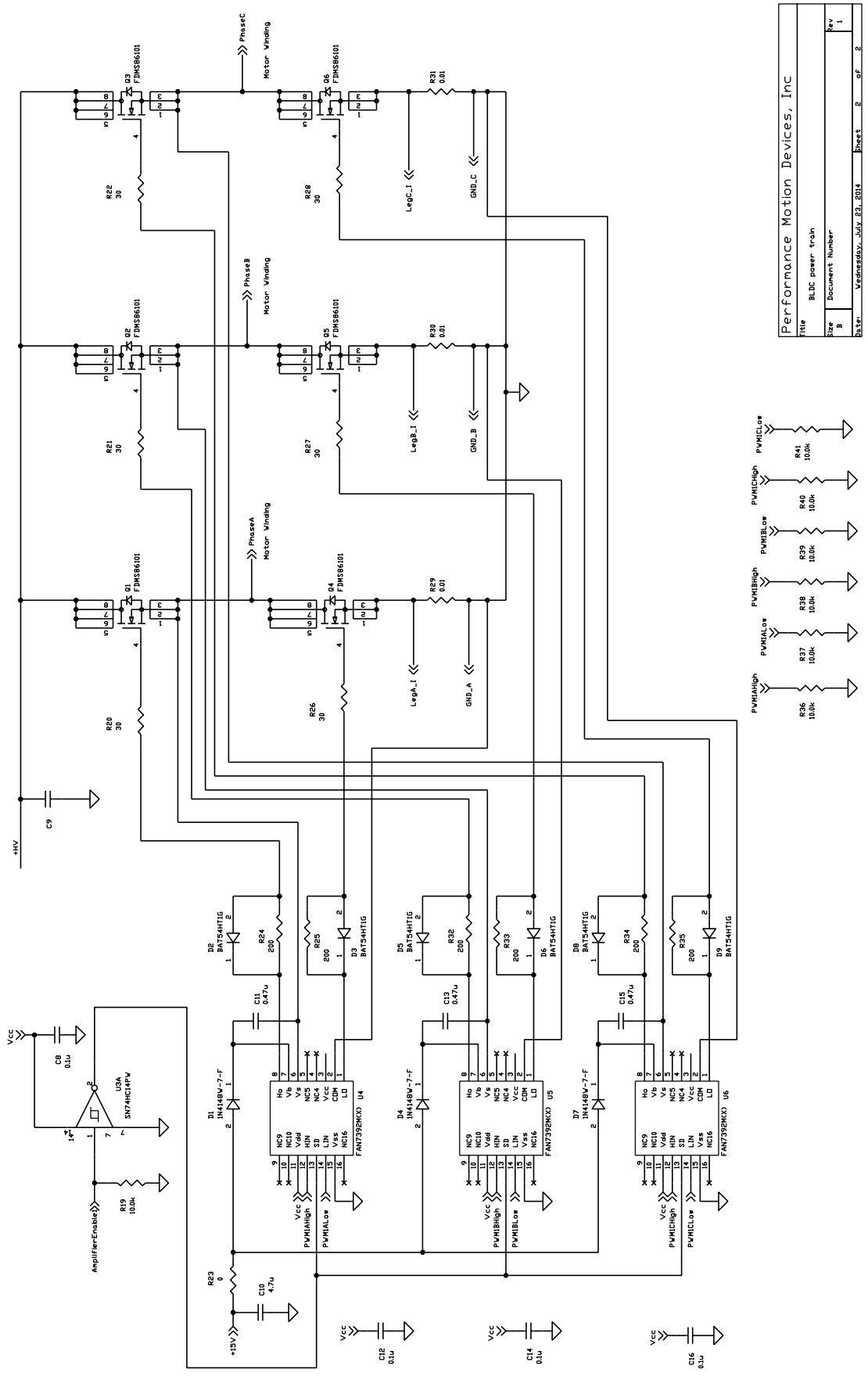


Figure 7-13: BLDC Motor Drive - Leg Current Sensing

Figure 7-14: BLDC Motor Drive - Power Train



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7.12.5 Brushless DC Motor Drive With Intelligent Power Module

Intelligent power modules integrate a power train, gate driver and protection circuitry into a single package. They have advantages of simply design, improved system reliability and fast time-to-market. This schematics show an example of a BLDC drive with an intelligent power module with current capability of 1A.

The module operates in the same way as the discrete solution as shown in previous sections. Please refer to the section on BLDC motor power train and step motor drive power train for details.

U2 has an internal temperature sensing output, V_{TS}. It can be connect to the MC58113's general ADC input and monitor this temperature. R16 and C13 is a low pass filter. D1 is for protection when V_{TS} output is higher than AnalogVcc.

Because intelligent power modules have control signals and a noisy power train in one package some special filters might be required. Please refer to the specific power module's user guide for details.

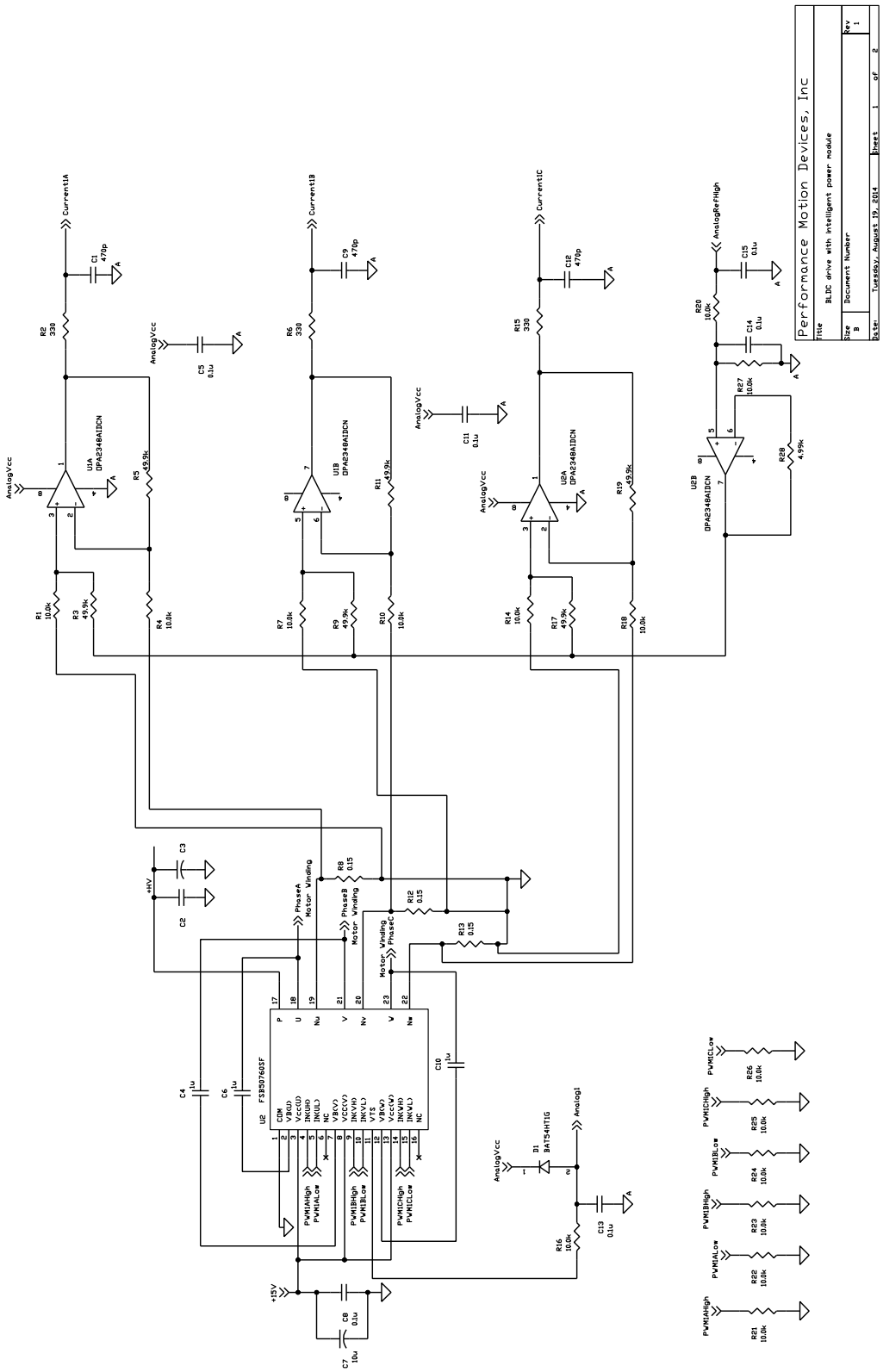


Figure 7-15: BLDC Drive with Intelligent Power Module

7.13 Dual DC Brush Motor Control Using Atlas Digital Amplifier

7.13.1 Atlas Power Input and Motor Output

Atlas is powered through pin pairs HV and Pwr_Gnd, and the power source is a transformer-isolated DC power supply. In this application the two Atlases share the same power supply. Alternatively they could be powered independently so that different motor voltages could be used.

For DC Brush motors pins MotorA and MotorB are wired to motor windings Motor+ and Motor-, respectively. Pins MotorC and MotorD are left un-connected.

Please refer to the *Atlas Digital Amplifier Users' Manual* for layout and wiring recommendations on power input and motor outputs.

7.13.2 Atlas SPI Interface

Atlas receives control commands through an SPI interface and functions as an SPI slave. Please refer to the *Atlas Digital Amplifier User Manual* for layout recommendation on SPI interface.

7.13.3 Atlas ~Enable and FaultOut Signals

Atlas has a dedicated input signal, *~Enable*, which must be pulled low for the Atlas output stage to be active.

FaultOut is a dedicated output. During normal operation it outputs low. When a fault occurs it will go into a high impedance state. In this example, FaultOut is pulled up by Vpullup through resistor R1. Vpullup can be up to 24V. Each Atlas may use a different Vpullup voltage, for example, if the fault signal is wired to a 5V TTL input, Vpullup can be 5V.

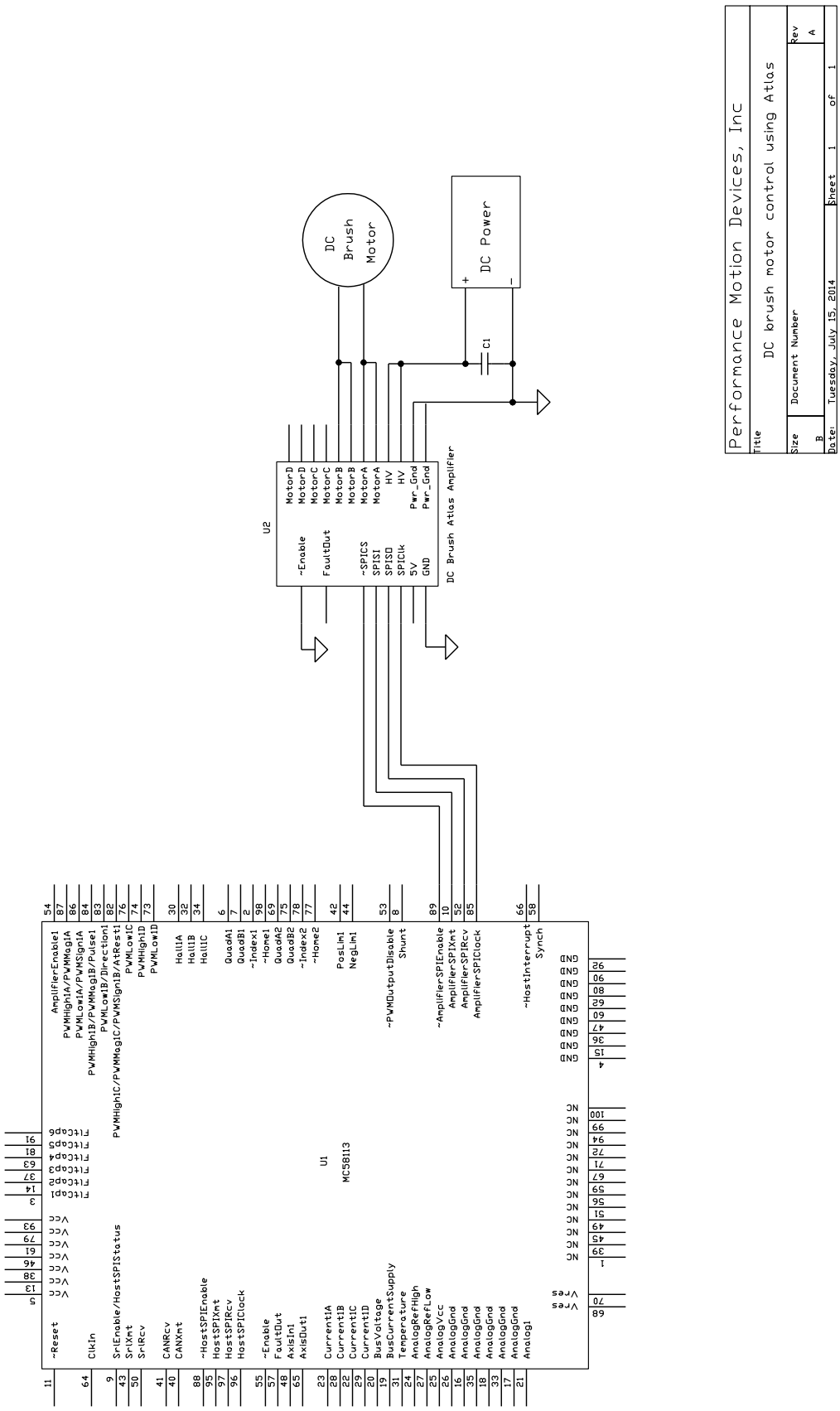


Figure 7-16: DC Brush Atlas with MC58113

7.14 DC Brush Motor Control Using SPI Interfaced DACs

The example in Figure 7-17 shows a solution for controlling DC brush motors using the MC58113's SPI interface to an Analog Devices 16-bit DAC AD1866. The AD1866 incorporates 5V CMOS logic with TTL compatible inputs, enabling a direct interface to the 3.3V MC58113 outputs. The Magellan SPI port can be configured using the **SetSPIMode** command to either falling edge without phase delay, or rising edge with phase delay, in order to maintain compatibility with the AD1866 SPI port. The AD1866 requires twos-complement data format which can be selected with the Magellan **SetOutputMode** command.

Note that only the 16-bit SPI DACs can be used with the MC58113. Many DACs come with the internal voltage reference feature. In the case that the external voltage reference is required, the user should choose the low-noise, low-drift high precision voltage source. For example, the TI REF50xx family reference chips provide a wide range of high precision voltage references from 2.5V to 10V.

7.14.1 Conditioning Circuitry

The AD1866 analog output, Vo, is a ±1Vpp output, ΔV, centered at the Vref = 2.5V reference voltage; in other words, Vo = Vref + ΔV. The AD1866 has moderate accuracy, with a mid-scale error of ±30 mV at ±3% of the full range, and a gain error of ±3% of the full range. The goals of the conditioning circuitry are to amplify the output to the ±10V range, and to provide a means to disable the AD1866 outputs until the MC58113 generates the first valid DAC word.

There are two methods for interfacing the AD1866 to a motor amplifier. First is when the output voltage is referenced to Vref, and the second is when it is referenced to the signal ground. The first solution is simpler, since it doesn't involve high precision matching resistors, but the appropriate method for a given application will depend on the requirements of the motor amplifier. Note that both interfaces use single-ended transmission. If the system requires differential transmission, then changes to the design will be required.

7.14.2 Referencing to Vref

An operational amplifier (U3) and two resistors (R_1 and R_2), are used to generate a ±10V differential output (V_{DAC}), which is referenced to Vref.

$V_{DAC} = -V \times (R_2/R_1) + Vref$, (1)

Selecting R2 = 100 k (%1) and R1 = 10.0 k (%1) results in an amplification gain of $A_M = 10$.

In order to avoid starting the motors in an unknown state at power-up, the DAC's output voltage is wired through a buffer equipped with shut-down capability. At power-up or reset, this buffer will be in shutdown mode resulting in high impedance output. In this state, the inverting x10 amplifier output will be Vref. Vref is wired through a buffer, since it is not designed to sink or source the large currents that may be required at the input stage of the motor amplifier.

Since the DAC performance poses no practical requirements on the op-amp selection, the selected components are the TLE2021, and dual TLV2473 with shutdown. The TLE2021 is capable of swinging up to the required worst-case +12.5+(0.6)V, but has a relatively large bias current. $R_3 = R_1 || R_2$ is used in order to reduce the effect of the bias current.

7.14.3 Referencing to AGND

By adding an additional resistor, R_4, and selecting $R_2 = R_4 = 100$ k (1%), and $R_1 = R_3 = 10.0$ k (1%), U3 becomes a differential amplifier with a nominal gain of 10.

$$V_{DAC} = - V \times R_2/R_1 \qquad (2)$$

This equation only holds true for matching pairs of resistors; otherwise undesired biases will not be completely canceled out, resulting in common-mode voltage. Using a 1% tolerant resistor will result in ~1% bias in the output signal. This bias is only one third of the AD1866 tolerances, but it should not be ignored. If this accuracy is not adequate, then high precision 0.1% resistors may be used. Alternately, the entire resistor set and amplifier may be replaced by a differential amplifier, such as the INA106 or the INA143, which offer a fixed gain of 10 and high CMRR.

A dual TLV2473 is used in order to ground the output at reset or power-up. The resulting circuitry forms an instrumental amplifier, which also benefits from the small output impedance of the buffers; thus minimizing the CMRR even further.

Notes:

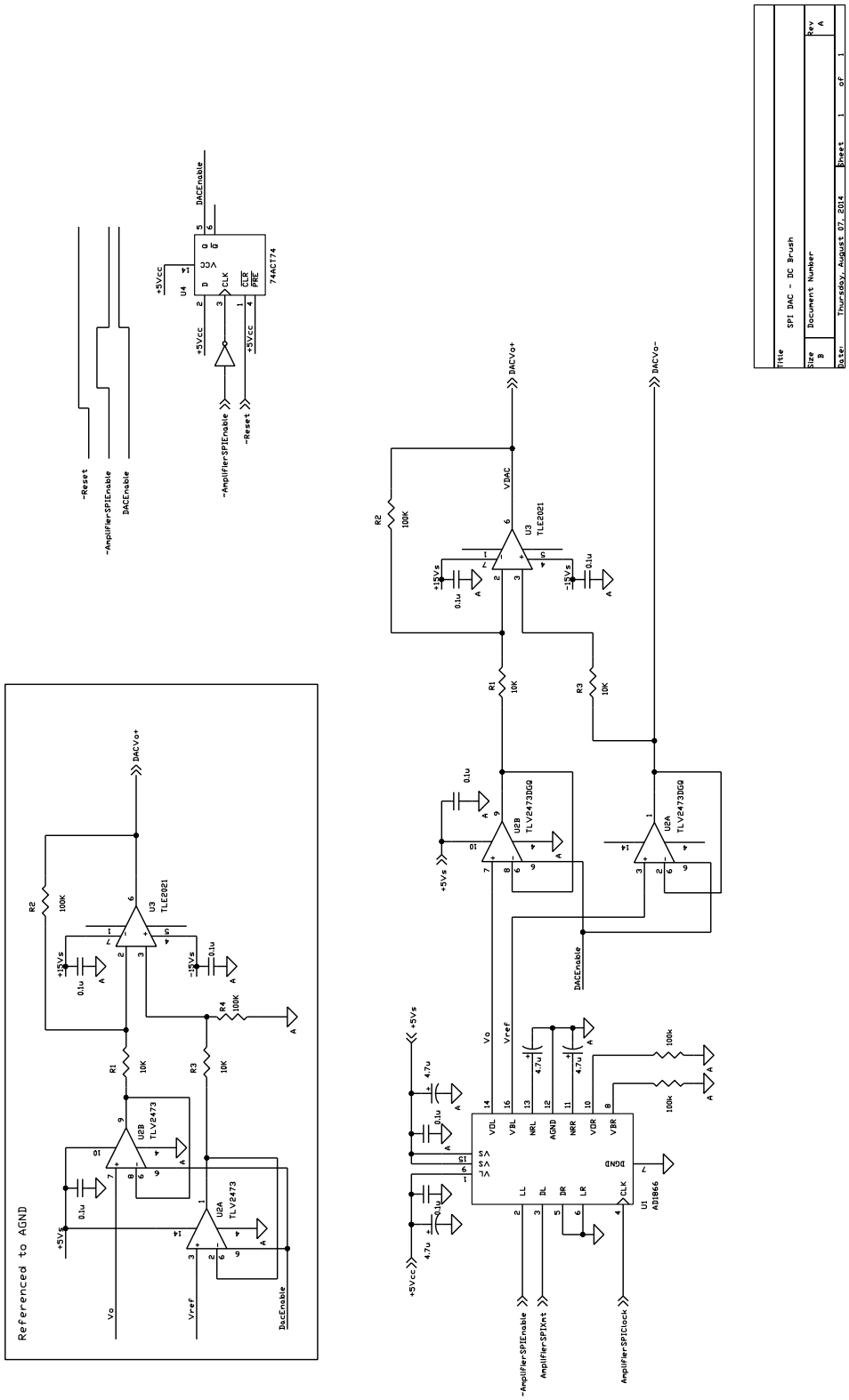
1 In both conditioning circuitries, an inverting amplifier (U6) is used. This may require that the motor output signal be inverted by setting bit 12 in the Magellan signal sense register.

2 The *DACEnable* signal goes active high on the first write to the DACs after the *~ResetHold* active low period has completed. Note that if the AD1866 is used to drive two motors, then the *DACEnable* signal should be generated with the use of the *SPIEnable* signal that corresponds to the last of the two motors being written to.

3 The AD1866 analog signal power supply should be decoupled with capacitors placed as closely as possible to both the supply pins and the signal ground. Refer to the AD1866 data sheet for a complete description.

4 The TLV2473 shutdown input accepts TTL input levels, which can be fed by a 3.3V CMOS D-FF. If other op-amps are selected, then the shutdown input levels should be checked. If there is level incompatibility the D-FF may be selected from the HCT/ACT family.

Figure 7-17: SPI DAC, DC Brush



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7.15 DC Brush, Brushless DC and Step Motor Drive using PWM Output

The MC58113 can drive DC brush, brushless DC, and step motors with the use of the PWM signals. The PWM magnitude is a symmetric, 10-bit resolution, 19.531 kHz signal. The supplies for the different motor drivers are not shown in the schematics, and it is assumed that the ground is isolated in order to prevent interference from low-signal components.

7.15.1 Using the ST L6234 to Drive Three-Phase Brushless DC Motors

In the following schematic, 50/50 PWM outputs are used to drive an L6234 three-phase motor driver. The TTL/CMOS input levels of the L6234 digital part are compatible with the outputs of the MC58113. If the power supply cannot sink the switching currents from the motor, a large capacitor should be added between the Vs input pin and ground. The schematic shows a 47 µF capacitor for a nominal 2A motor. To detect malfunctions, the *Vsense* signal may be used to sense the amount of current flowing through the motor windings.

The circuitry provided in this section does not provide active current control. See Section 7.12, "PWM High/Low Motor Drive With Leg Current Sensing/Control," for PWM-based application examples using the MC58113 IC that provide active current control.

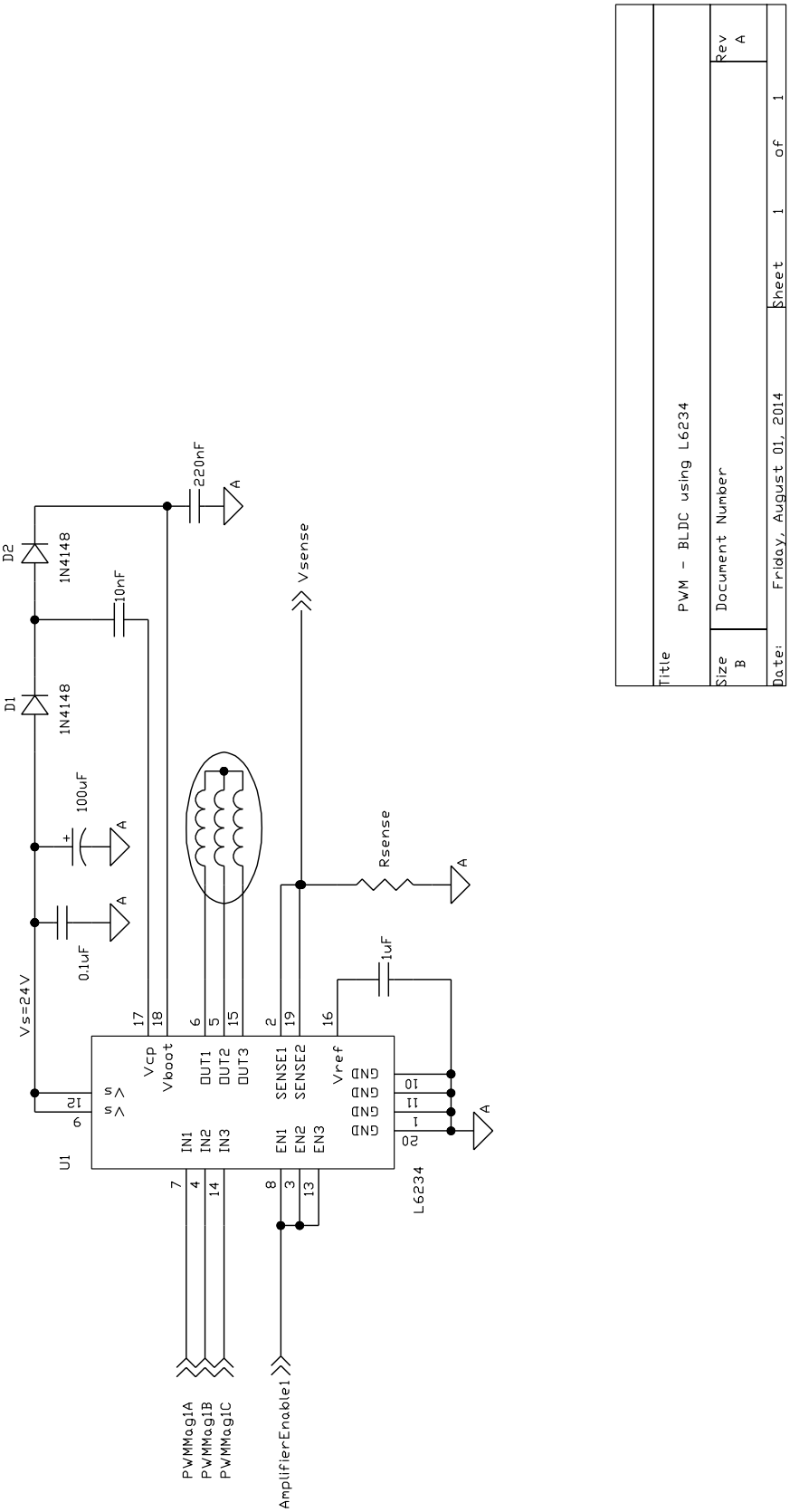


Figure 7-18: BLDC Amplifier Using L6234

7.15.2 Using the TI LMD18200 to Drive DC Brush Motors

In the following schematic, a magnitude and direction *PWM* signal is used to drive a DC brush motor with a nominal 24V, 2A drive. The H-bridge driver selected for this task is the LMD18200, which can be driven directly from a 3.3V CMOS logic output and as such can be directly interfaced to the MC58113.

There are two methods in which the output current of the H-bridge may be controlled.

First, in the *locked anti-phase control* mode (see the LMD18200 data sheet), a 50/50 *PWM* signal is applied to the LMD18200 DIR input, while the PWM input is tied high. The current ripple in this mode is relatively high, as the circulating currents are quickly decaying.

Second, in *the sign/magnitude control* mode, sign and magnitude *PWM* signals are applied to both the PWM and DIR inputs of the LMD18200. In this mode, the resultant current ripple is reduced resulting in smoother operation of the motor. When the acceleration/deceleration requirements for the motor are not high, the sign/magnitude PWM control mode is preferred. This method is demonstrated in the example.

The LMD18200 is equipped with an internal overcurrent circuit, which is tuned to a 10A threshold. External over-current circuitry may be added for currents with a lower threshold by using the sense output. In order to detect malfunctions, the *Vsense* signal may be used to sense the amount of current flowing through the motor windings. The sense output of the LMD18200 samples only a fraction of the drive current, with a typical 377 µA sensing per 1A driving current. .

Note that the circuitry provided in this section does not provide active current control. See Section 7.12, "PWM High/Low Motor Drive With Leg Current Sensing/Control," for PWM-based application examples using the MC58113 IC that provide active current control.

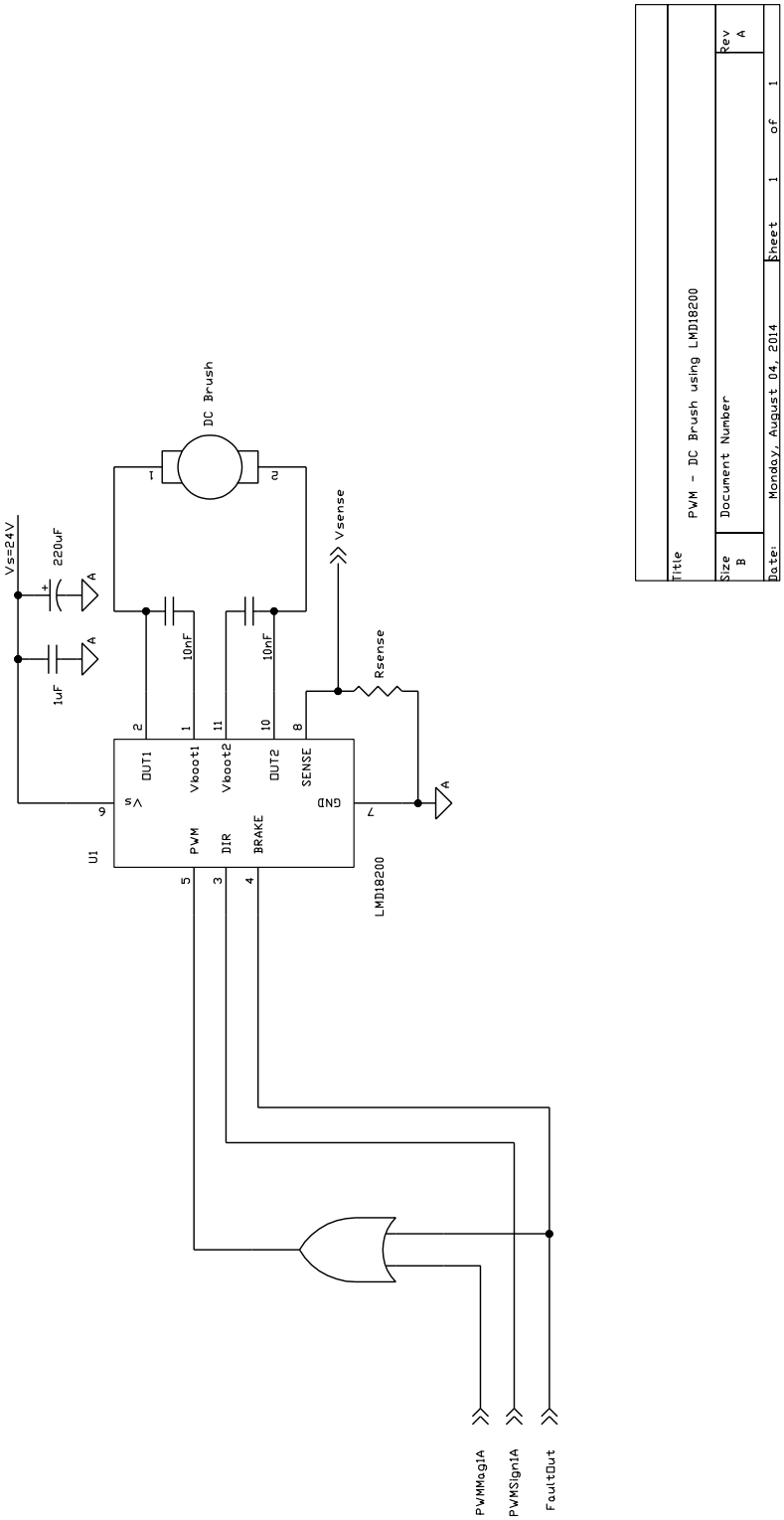


Figure 7-19: DC Brush Amplifier Using LMD 18200

7.15.3 Using the ST L6202 to Drive Step Motors

In this example a pair of ST L6202 H-bridges are used to drive a two-phase microstepping motor in voltage-control mode, with the following nominal values: Vs = 24V, Imax = 2A. Two schematics are shown (Figure 7-20 and Figure 7-21), which utilize different decay current methods.

The first schematic uses fast decay mode, and in the second schematic, mixed-decay mode is used. Decay mode refers to the manner in which circulating currents in the motor windings are directed in the H-bridge. Fast decay is usually the preferred choice when a fast response is needed. When attempting to quickly decrease the current through the winding, it is beneficial to use the fast decay mode. Slow decay is desirable as long as the current through the winding tracks the commanded waveform, since slow decay will result in lower power dissipation in the motor and smoother motion. In a mixed decay mode, both types of the decay modes are used. For example, slow decay is used when increasing the current in the winding, and fast decay is used when decreasing the current in the winding.

The ST L6202 is an H-bridge, with separate controls for each of its halves (IN1 and IN2). In Figure 7-20, the MC58113 motion control IC is configured for the PWM High/Low output mode. The *PWMHigh1A, PWMLow1A, PWMHigh1B* and *PWMLow1B* signals are applied to these inputs which will result in fast decay mode operation.

In Figure 7-21, PWM magnitude signals are applied to the inputs to demonstrate the mixed decay mode operation. When L6202's internal source drivers are both disabled and both sink transistors are turned on, the load inductance causes the current to recirculate through the sink drivers. This will result in slow decay mode operation. The MC58113 motion control IC is configured for the PWM Magnitude/Sign output mode. *PWMMagA is* being offset to (in advance of) *PWMMagB* by 90 degrees. *PWMMagC* is used to generate an additional PWM magnitude signal *XMagA/B*. A decay mode indicator *FastA/SlowB* is generated from the *PWMSignA* and *PWMSignB* signals by using XOR logic gates and a D flip-flop. When the *FastA/SlowB* signal is logic high, it indicates that Phase A is in the fast decay mode and Phase B is in the slow decay modes respectively. When the *FastA/SlowB* signal is logic low, it indicates that Phase A is in slow decay mode and Phase B is in the fast decay modes respectively.

The following table shows the logic which generates the input signals to the L6202 H-bridge, IN1 and IN2, as a function of *FastA/SlowB*, *PWMSignA*, and *PWMSignB* signals. In the reference schematic the logic is implemented using a pair of 74AC153 dual 4-to-1 multiplexers. More efficient designs may be derived by exploiting the inter-relations of the different signals. The propagation delay through the logic should be kept as small as possible to reduce delays between the two phases and to reduce asynchronous effects.

		Phase A			Phase B	
FastA/SlowB	**PWMSignA**	**IN1**	**IN2**	**PWMSignB**	**IN1**	**IN2**
1 (FastA, SlowB)	0	Mag1A	~Mag1A	0	L	XMag1B
0 (SlowA, FastB)	0	L	XMagA	1	Mag1B	~Mag1B
1 (FastA, SlowB)	1	~Mag1A	1	1	XMag1B	L
0 (SlowA, FastB)	1	L	0	0	Mag1B	~Mag1B

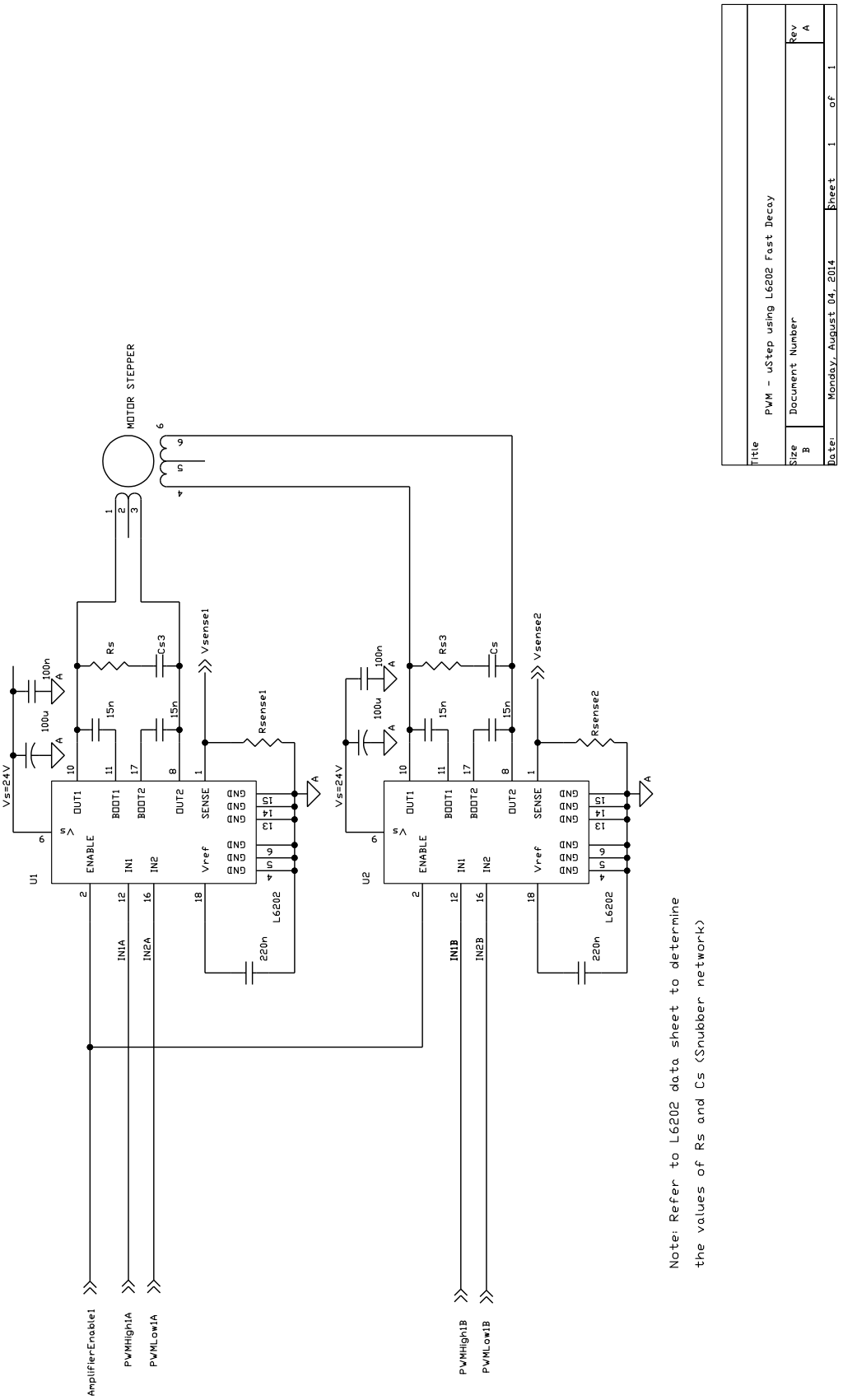
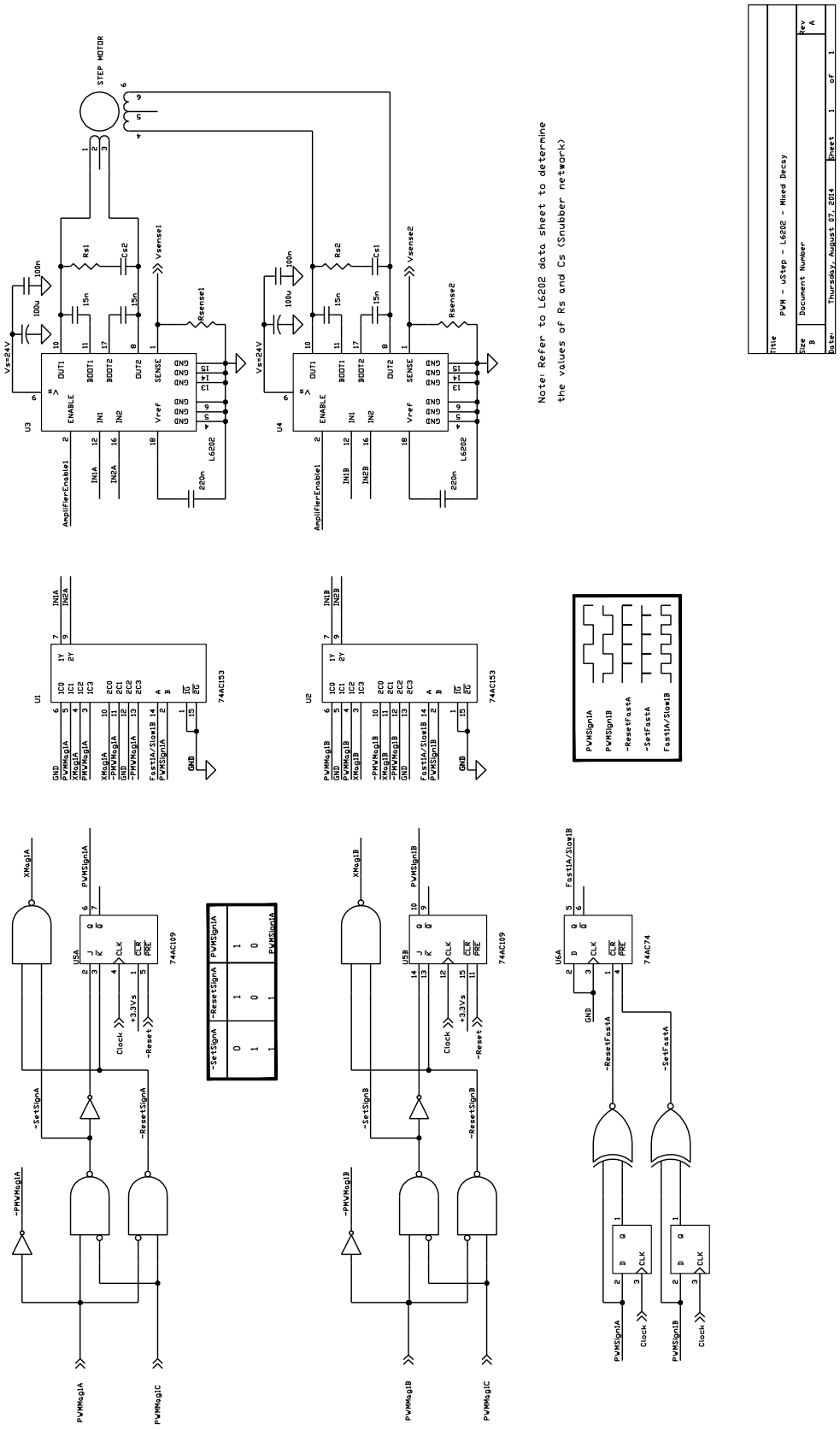


Figure 7-20: Microstep Amplifier Using L6202, Fast Decay

Figure 7-21: Microstep Amplifier Using L6202, Mixed Decay



7.15.3.1 SignA/SignB Signal Generation

In order to generate the sign signals, the *PWMMagA/B* signals are compared against the 50% duty-cycle reference signal, *PWMMagC*. £ *ResetSign* and *~SetSign* are active low when the reference signal is wider or narrower than the *PWMMag* signal, respectively. These signals are synchronized by the MC58113 10MHz input Clock. Figure 7-21 shows the sign signal state during each phase of the motor output waveform.

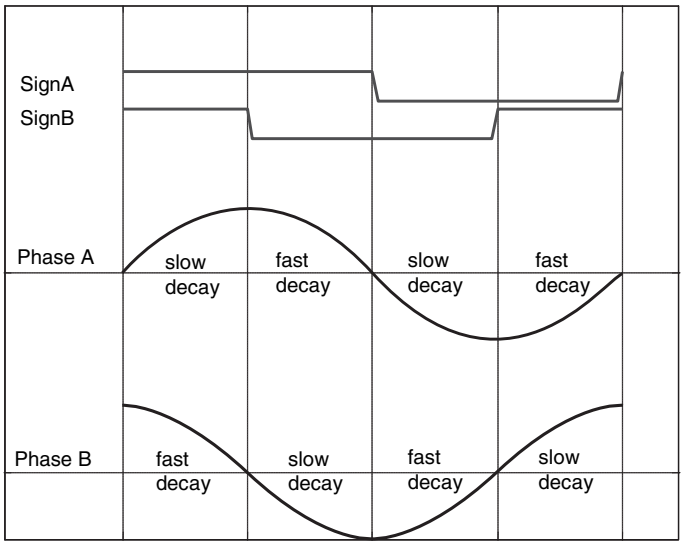


Figure 7-22: Signal State During Each Phase of Motor Output Waveform

7.15.3.2 LPF Design

The *PWM* signal generated by the MC58113 has an 80 kHz cycle. With 256 resolution steps of 50 µsec each, it can encode sine waveform frequencies up to 500 Hz.

Figure 7-23 shows the spectra of the *PWM* signal encoded with a 150 Hz electrical cycle signal, superimposed with an ideal analog 150 Hz absolute magnitude sine wave (red). The *PWM* signal possesses energy at the PWM cycle frequency and its higher order harmonics. This energy is related to the PWM encoding waveform, which should be filtered out; the non-filtered portion of it will appear as ripple. The LPF goal is to pass the energy of the encoding signal, while suppressing the PWM waveform contributions.

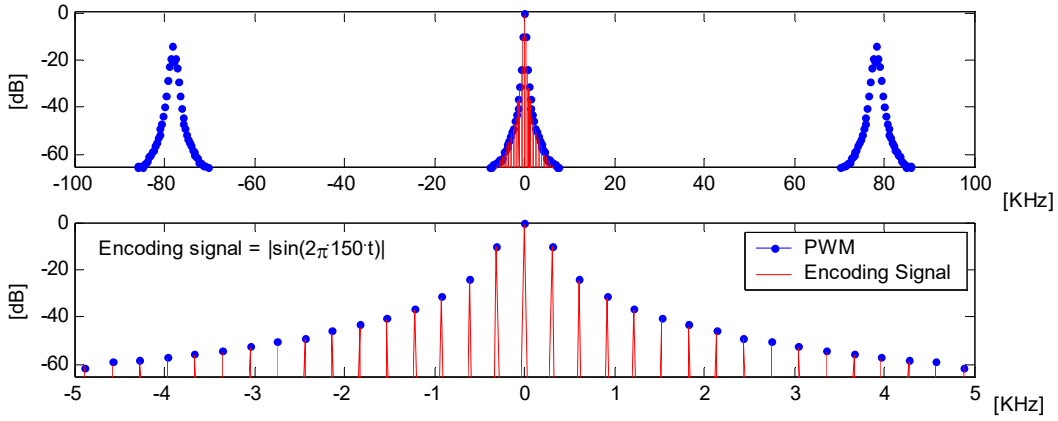


Figure 7-23: Encoded PWM Signal Spectra

Based on this figure, the filter should have a cut-off frequency at 5 kHz, and suppression of at least 40 dB at 78 kHz.

A second order passive filter is adequate for this task, as indicated in the following figures. Figure 7-24 shows a second-order RC filter frequency response, and Figure 7-24 shows the filter's output for an ideal 150 Hz electrical cycle PWM input.

Figure 7-24: Filter Frequency Response

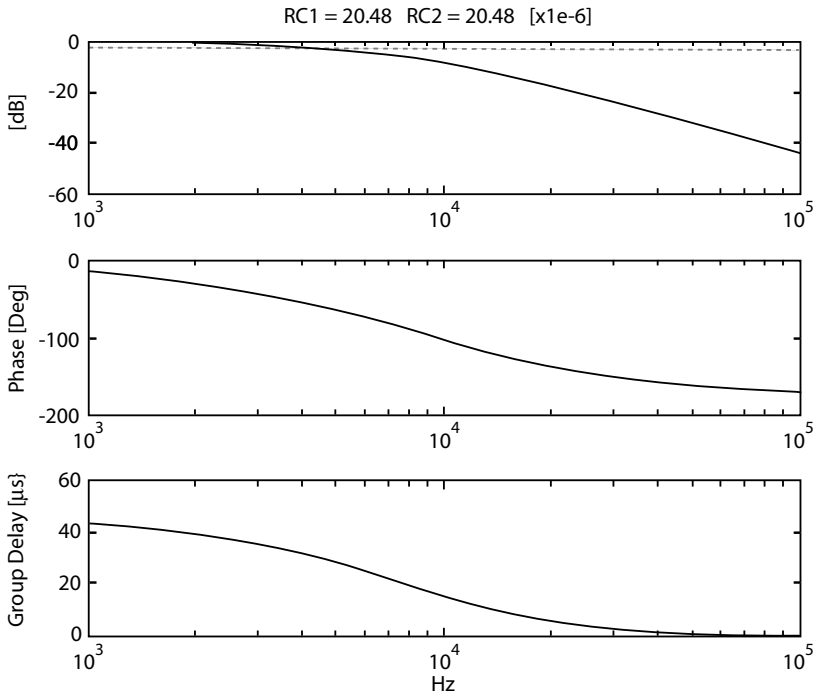
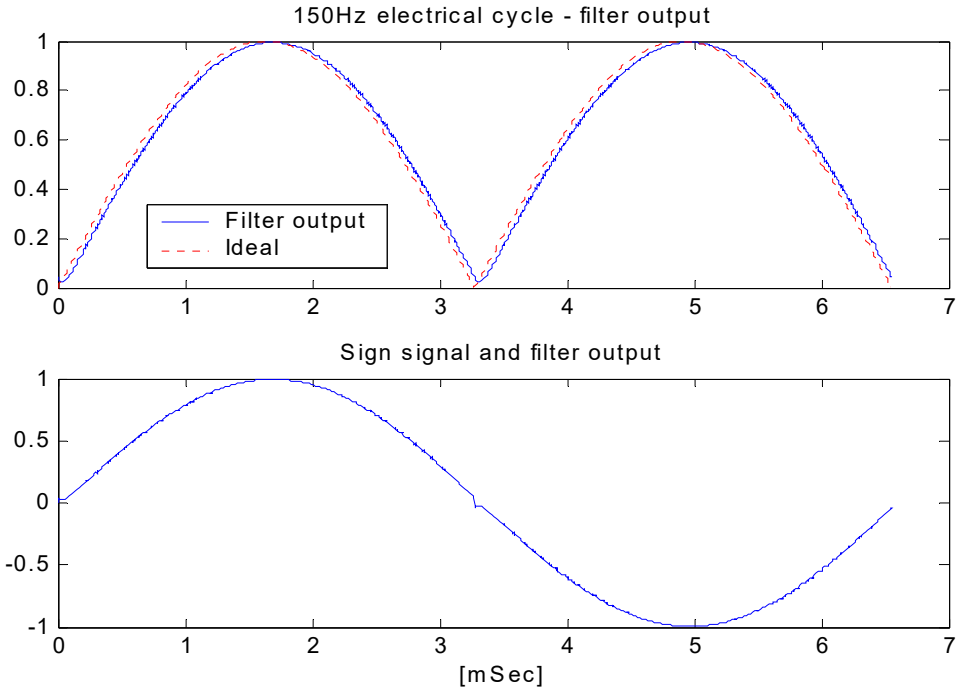


Figure 7-25: Filter Output to 150 Hz Electrical Cycle



If a different filter is to be designed, the following points should be considered.

1. Reducing the cut-off frequency will result in a larger imperfection at the zero crossing point due to:

   a. The filtered curve at the zero crossing points will experience higher levels.

   b. The filter group-delay will be larger; thus increasing the mismatch between the sign signal and the filtered signal. This can be remedied by delaying the sign signal according to the filter group delay.

2. Increasing the cut-off frequency will reduce the suppression of the PWM waveform, resulting in larger ripple.

3. Increasing the order of the RC filter will result in a better waveform. Due to the slow roll-off of the filter, the improvement will probably be insignificant.

7.16 Using the Allegro A3977 to Drive Microstepping Motors

The A3977 is a complete microstepping motor driver with a built-in translator. The translator is capable of driving bi-polar stepper motors in full-, half-, quad-, and eighth-step modes. When the step input transitions from low to high, the A3977 will advance the motor one full-, half-, quad-, or eighth-step according to the configuration of the MS1 and MS2 pins. In the example the driver is configured for eighth-step resolution.

The A3977 operation can be tuned with the use of external components. *CT* is used to determine the blanking period of the current sense comparator circuitry. The product of *RT* and *CT* is used to determine the PWM constant off period. *R1* and *R2*, along with *RT* and *CT*, determine the percentage of the fast decay in mixed decay mode. The sense resistors, *Rsense*, should be selected according to the maximum current and voltage restrictions of the driver. Refer to the device data sheet for further information.

For a direct interface of the pulse signal to the step input, the polarity of the pulse signal must be inverted using the **SetSignalSense** command. This is required because the A3977 recognizes a step during a low-to-high transition of the step input signal, whereas the non-inverted behavior of the MC58113 is to generate a step on a high-to-low transition.

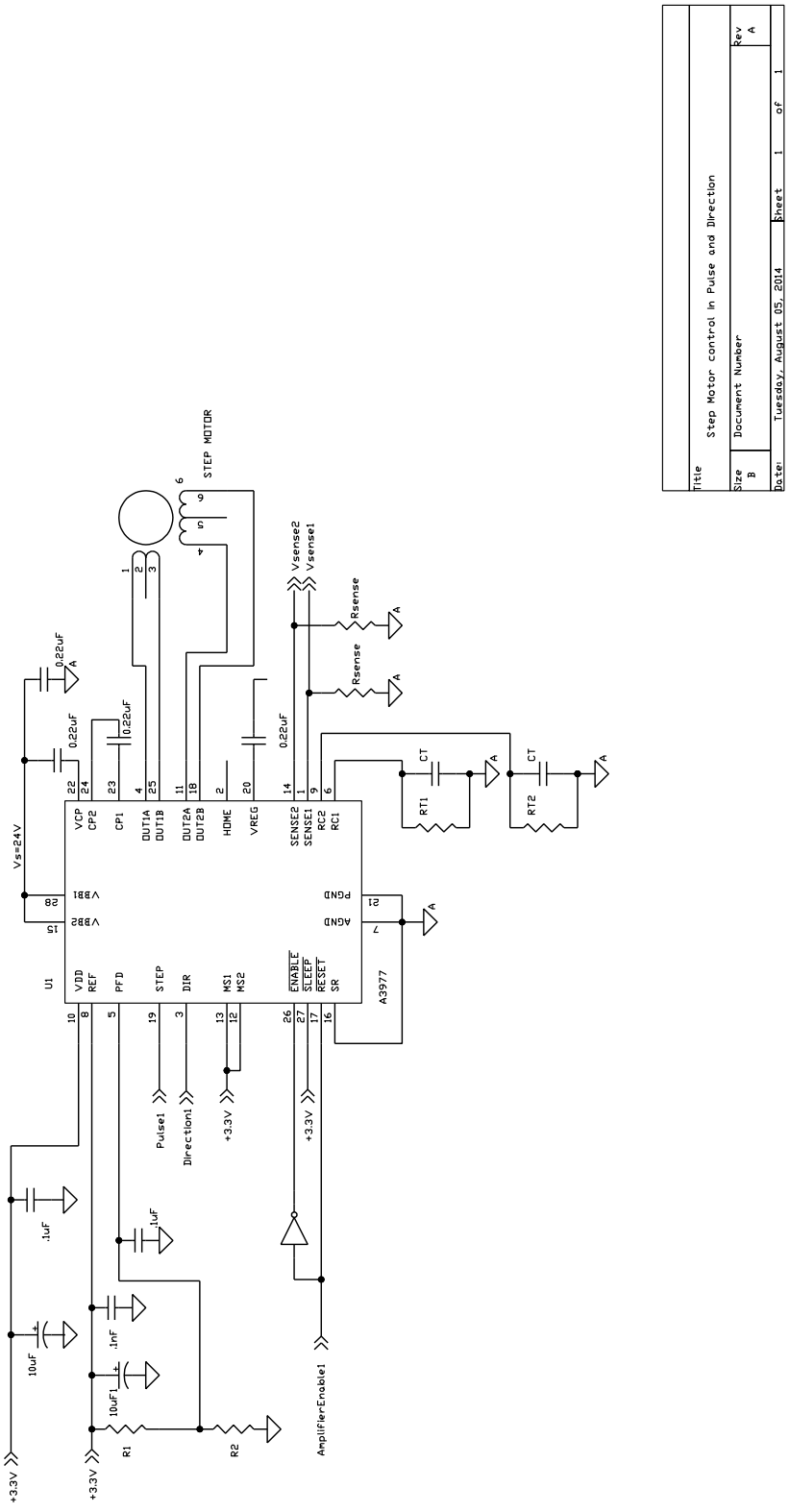


Figure 7-26: Step Motor Amplifier Using Allegro A3977

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For additional information, or for technical assistance, please contact PMD at (978) 266-1210.

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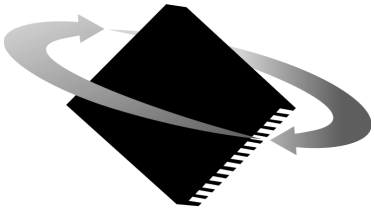

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